

Electrical, Electronics and communications, and Computer Engineering

Reliability Analysis of Multibit Error Correcting Coding and Comparison to Hamming Product Code for On-Chip Interconnect

Asaad Kadhum Chlaab *
MSc student
Collage of Engineering,
University of Baghdad
Baghdad, Iraq
asaadkadumch@gmail.com

Wameedh Nazar Flayyih
Lecturer Professor
College of Engineering,
University of Baghdad
Baghdad, Iraq
wam.nazar@coeng.uobaghdad.edu.iq

Fakhrul Zaman Rokhani
Assistant Professor
System-on-Chip Research Center
Universiti Putra Malaysia,
Serdang 43400, Malaysia
fzr@upm.edu.my

ABSTRACT

Error control schemes became a necessity in network-on-chip (NoC) to improve reliability as the on-chip interconnect errors increase with the continuous shrinking of geometry. Accordingly, many researchers are trying to present multi-bit error correction coding schemes that perform a high error correction capability with the simplest design possible to minimize area and power consumption. A recent work, Multi-bit Error Correcting Coding with Reduced Link Bandwidth (MECCRLB), showed a huge reduction in area and power consumption compared to a well-known scheme, namely, Hamming product code (HPC) with Type-II HARQ. Moreover, the authors showed that the proposed scheme can correct 11 random errors which is considered a high number of errors to be corrected by any scheme used in NoC. The high correction capability with moderate number of check bits along with the reduction in power and area requires further investigation in the accuracy of the reliability model. In this paper, reliability analysis is performed by modeling the residual error probability P_{residual} which represents the probability of decoder error or failure. New model to estimate P_{residual} of MECCRLB is derived, validated against simulation, and compared to HPC to assess the capability of MECCRLB. The results show that HPC outperforms MECCRLB from reliability perspective. The former corrects all single and double errors, and fails in 5.18% cases of the triple errors, whereas the latter is found to correct all single errors but fails in 32.5% of double errors and 38.97% of triple errors.

Key Words: error correction codes, multi bit error, on chip interconnect, residual error rate.

*Corresponding author

Peer review under the responsibility of University of Baghdad.

<https://doi.org/10.31026/j.eng.2020.06.08>

2520-3339 © 2019 University of Baghdad. Production and hosting by Journal of Engineering.

This is an open access article under the CC BY4 license <http://creativecommons.org/licenses/by/4.0/>.

Article received: 17/12/2019

Article accepted: 8/2/2020

Article published:1/6 /2020



تحليل موثوقية ترميز تصحيح الاخطاء المتعددة ومقارنة مع ترميز ضرب هامنج من أجل الروابط على الرقاقة

فخر الزمان روخاني
استاذ مساعد دكتور
جامعة بوترا ماليزيا - مركز أبحاث الأنظمة على الرقاقة

وميض نزار فليح
مدرس (دكتور)
جامعة بغداد- كلية الهندسة

اسعد كاظم جلاب
طالب ماجستير
جامعة بغداد- كلية الهندسة

الخلاصة

أصبحت أنظمة التحكم في الأخطاء ضرورية الاستعمال في الشبكة على الرقاقة (NoC) لغرض تحسين الموثوقية حيث ازدادت الأخطاء الواقعة في الروابط على الرقاقة مع التقلص المستمر للأبعاد الهندسية. وفقاً لذلك، يحاول العديد من الباحثين تقديم أنظمة ترميز تصحيح الأخطاء المتعددة ذات قدرة تصحيح عالية للخطأ مع أبسط تصميم ممكن لتقليل استهلاك المساحة المشغولة والطاقة. يظهر عمل حديث، وهو ترميز تصحيح الأخطاء المتعددة مع عرض نطاق ترددي منخفض للوصلة (MECCRLB)، انخفاضاً كبيراً في المساحة المشغولة واستهلاك الطاقة مقارنة بنظام مشهور هو (Hamming product code (HPC) with Type-II HARQ). ويوضح المؤلفون أيضاً أن الترميز المقترح يمكن أن يصحح 11 خطأ عشوائياً والذي يعتبر عدداً كبيراً من الأخطاء التي يمكن تصحيحها بواسطة أي ترميز مستخدم في ال (NoC). القدرة التصحيحية العالية مع عدد معتدل من وحدات التحقق إلى جانب التقليل الحاصل في الطاقة والمساحة المشغولة يتطلب المزيد من التحقيق في دقة النموذج الرياضي. في هذا البحث يتم تحليل الموثوقية من خلال ايجاد نموذج رياضي يمثل احتمالية الخطأ المتبقي الذي يمثل احتمال حدوث خطأ أو عطل في وحدة فك الترميز. تم اشتقاق نموذج جديد لتقدير احتمالية الخطأ لـ MECCRLB، والتحقق من صحته بمقارنته بالمحاكاة ثم مقارنته بـ (HPC) لتقييم قدرة MECCRLB التصحيحية. تبين النتائج ان HPC يقدم مستوى موثوقية اعلى من MECCRLB. الاول يصحح كل الاخطاء الاحادية و الثنائية ويفشل في 5.18% من حالات الاخطاء الثلاثية، بينما الاخير يصحح كل الاخطاء الاحادية لكن يفشل في 32.5% من الاخطاء الثنائية و 38.97% من الاخطاء الثلاثية. الكلمات الرئيسية: رموز تصحيح الخطأ، خطأ بتات متعددة، الروابط على الرقاقة، معدل الخطأ المتبقي .

1. INTRODUCTION

On-chip communication between the many components integrated on a single chip is facing many reliability issues along with the stringent area and power constraints. On-chip interconnect errors caused by many effects including supply voltage fluctuation, crosstalk, process variation, radiation, or electromagnetic interference become increasingly problematic in very deep submicron (VDSM) technology (Sridhara and Shanbhag, 2005). Reliability can be improved by applying error control techniques, such as automatic repeat request (ARQ), forward error correction (FEC), and hybrid ARQ (HARQ) to on-chip interconnects. Single-error correcting (SEC) codes (e.g., Hamming) have been widely used in previous works to address transient errors. With the increasing probability of multiple random and burst errors in VDSM technology more powerful and efficient error control schemes were needed (Bertozzi and Benini 2005). Accordingly, many error controls schemes for multi-bit error correction appeared to increase the error correction bound. In Combined Crosstalk Avoidance Code with Error Control Code (Joint LPC- CAC-ECC) the use of simple parity calculation along with message triplication make the correction of two random errors and some of three is possible (Kummary and Dananjayan, 2019). While in Joint crosstalk avoidance and Triple Error Correction (JTEC), Hamming code with message duplication is used to correct three errors. Further optimization was applied for this scheme yielding Triple Error Correction and Quadruple Error Detection (JTEC-SQED) (Ganguly and Pande, 2009). Another optimization made In Joint Crosstalk Aware Multiple Error Correction (JMEC) to correct adjacent errors the used of changed interleaving distance between adjacent bits makes the correction of nine adjacent errors possible (Gul and Chouikha, 2017) Duplication with two dimensional parities was also proposed to provide up to seven errors detection (Flayyih and Samsudin, 2014) or six errors detection and single error correction



(Flayyih and Samsudin, 2020). In Multi Bit Random and Burst Error Correction (MBRBEC) the use of extended Hamming code with triplication can raise the correction capability to five errors (Maheswari and Seetharaman , 2013). while in Quintuplicated Manchester error correction (QMEC) the nonuple errors correction is possible (Narayanasmy and Muthurathinam,2018). All these duplications, triplication and quintuplication based coding schemes provide high error control at the cost of high link size. Another group of coding schemes provide multibit error control without high link size overhead. Both multiple random and burst errors were corrected by Hamming product codes (HPC) (Fu, 2009,) where extended hamming product code (HPC) combined with type-II HARQ for was used for correcting up to five errors. Type-II HARQ was adopted to avoid the high link size overhead by sending the message in two steps. A recent research, (Vinodhini and Murty, 2018,.) proposed multi-bit error correcting coding with reduced link bandwidth (MECCRLB) code. The authors try to reduce the area and power consumption by using different product code arrangements by applying hamming coding on rows and a simple parity on columns. The authors show huge reduction in area and power consumption as compared to(Fu ,2009). They show that their method can correct burst errors of four bits or random error of eleven bits which resulted in lower probability of residual error rate which means higher reliability. All these error correction techniques can correct multi-bit errors with different error correction capability. Besides the correction capability, two important metrics are considered when evaluating the different coding techniques, namely the circuit design complexity and the required link size to send the codeword. These metrics reflect the area and power consumption which are critical in VLSI designs. The reliability provided by any coding scheme is evaluated by the residual error probability which is a measure of the failing probability of the coding scheme. To provide an easy way for comparing the coding schemes, mathematical models are derived to estimate the residual error probability. The models are essential in evaluating the reliability and also in finding the required link voltage swing to achieve a certain reliability level. Thus, the accuracy of these models is reflected in the reliability level accuracy and in the selected voltage swing.

The high error correction capability of MECCRLB with low number of parity bits required along with the reduced circuit complexity motivates the requirement of further analysis of this scheme to verify its higher reliability level compared to HPC. This is supported by the fact that correction capability is upper limited by the Hamming distance emerging from the data redundancy. The main contribution of this paper is the derivation of an accurate residual error probability model to estimate the MECCRLB reliability and compare it to HPC (Fu, 2009). supported by simulation results.

The remaining of the paper is arranged as follows: the literature review for related works are presented in Section 2. In Section 3, reliability analysis is done for the considered works, while in Section 4, the results and discussion are presented. Eventually, Section 5 represents the conclusion.

2. LITERATURE REVIEW

To analyze the reliability of the two error coding schemes; hamming product code with type-II HARQ Fu ,2009 and MECCRLB Vinodhini and Murty,2018, the message arrangements are first introduced along with the encoding and decoding in each scheme

2.1-Extended Hamming Product Code with type II HARQ

The k bit input message is arranged into a $(k_1 \times k_2)$ matrix as shown in Fig. 1. The number of rows, k_2 , is always chosen to be four to reduce the link size according to the study done in (Fu, 2009). Row parity check bits are obtained by encoding the (k_1) bits in each row using extended Hamming row encoder $EH(n_1, k_1)$, where n_1 is the row encoded word size. Column parity check bits are

obtained by encoding the (k_2) column bits using column encoder EH (n_2, k_2) , where n_2 is the column encoded word size. Checks-on-checks can be generated by encoding the column parity check bits using row encoder. In (Fu 2009), the authors used extended Hamming Product Code with type II HARQ to reduce the number of interconnection links. The encoder first encodes the k_2 rows using extended Hamming code and sends the result to the decoder encompassing separate row decoders that correct single error and detect double errors at each row. If errors occur and they are within the error correction capability of the decoder, then there is no need to send the column parities and checks on checks. If the errors are detectable but uncorrectable the decoder will request the extra column parity check bits along with checks on checks bits to be sent to correct the detectable errors where each column encoder can also correct one error and detect two. Thus, the second transmission is to increase the correction capability. A message with 32-bits is arranged as (8×4) matrix. Each row is encoded as EH $(13,8)$ resulting in 52-bit message. Each column is encoded as EH $(8,4)$ resulting in 32-bit that will be further encoded using row encoder EH $(13,8)$ to generate checks on checks leading to 52-bit message saved in a buffer and sent in case of NACK.

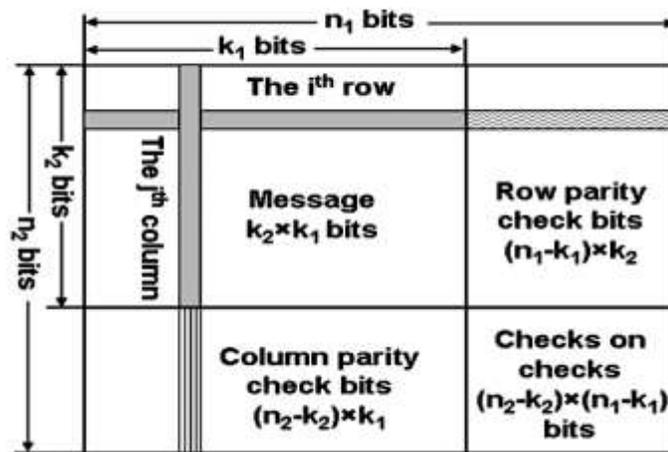


Figure 1. 2-D product codes Fu, 2009.

2.2 MECCRLB Code

In this coding scheme the k bits input message is arranged with $k_2=3$ rows and number of columns $(k_1 = k/3)$. The extended hamming product is applied to the three rows only, while simple parity is applied to the columns. Fig.2 shows a 32-bit message where G1 to G3 are fed to extended hamming code encoder while simple parity checks will be calculated for vector 1 to vector 10. For 32-bit message G1 and G2 are encoded using EH(16,11) while G3 is encoded using EH(15,10), thus, the size of the encoded message will be 57-bits. MECCRLB code was proposed to reduce the complexity of circuits used in HPC Type-II HARQ and also to send the data in one transmission by reducing the number of parities.



X1	X4	X7	X10	X13	X16	X19	X22	X25	X28	X31	G1
X2	X5	X8	X11	X14	X17	X20	X23	X26	X29	X32	G2
X3	X6	X9	X12	X15	X18	X21	X24	X27	X30		G3

X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	X12	X13	X14	X15
vector1			vector2			vector3			vector4			vector5		
X16	X17	X18	X19	X20	X21	X22	X23	X24	X25	X26	X27	X28	X29	X30
vector6			vector7			vector8			vector9			vector10		

Figure 2. 32-bit input message divided into three groups and ten vectors (Vinodhini and Murty ,2018).

Unlike HPC the encoder will send the whole encoded message. The decoder will correct the errors within its correction capability according to Fig.3 which shows the decoder correction algorithm.

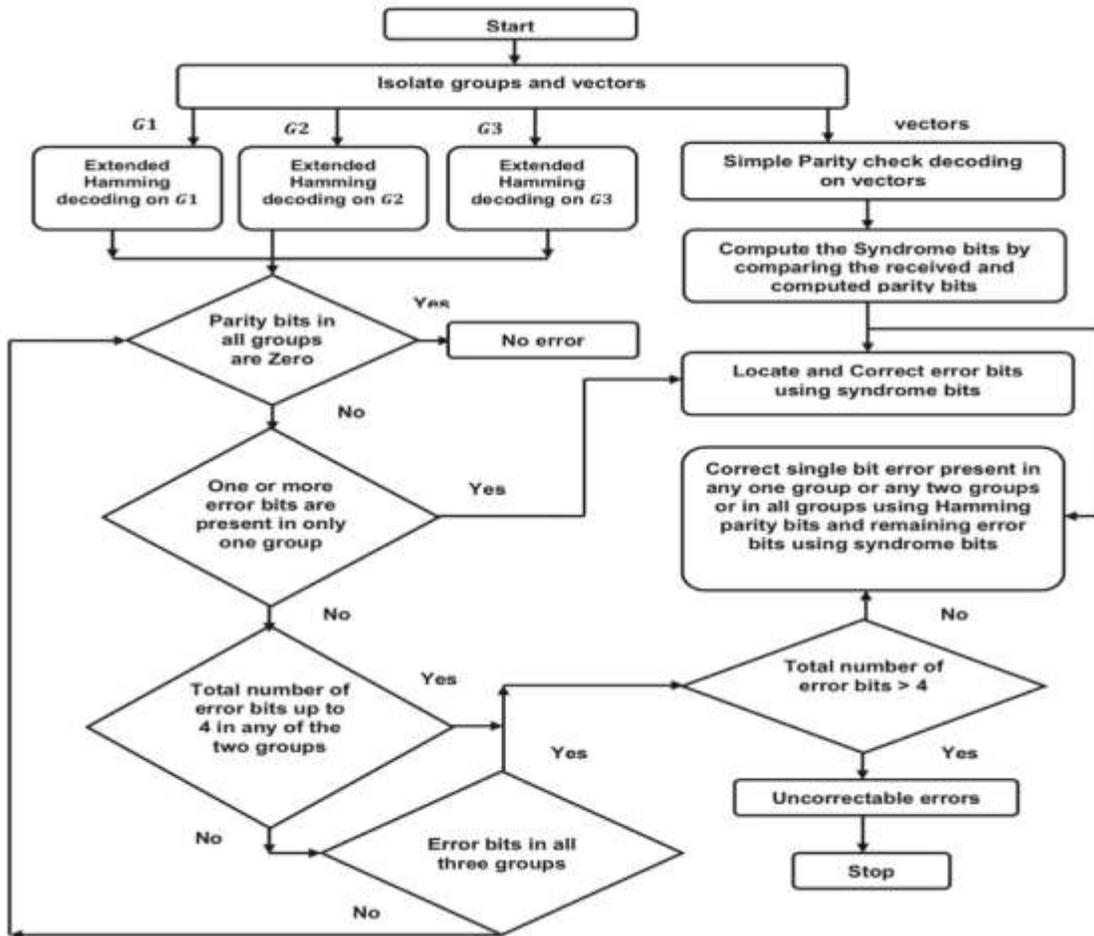


Figure 3. MECCRLB decoder algorithm Vinodhini and Murty ,2018.



3. RELIABILITY ANALYSIS

Reliability can be measured by calculating the residual error probability ($P_{residual}$), which represents the probability of decoder error or failure; this is a complement to the probability of proper decoding which is the sum of the probabilities of correcting random errors and burst errors. The relationship between probability of residual error ($P_{residual}$) and probability of proper decoding (P_{pd}) is given in **Fu and Ampadu,2008** as:

$$P_{residual} = 1 - P_{pd} \quad (1)$$

In the following subsections, **Fu,2009** and **Vinodhini and Murty ,2018** will be analyzed for random errors only, since both coding schemes can correct acceptable amount of burst errors, namely six in **Fu,2009** and four in **Vinodhini and Murty, 2018**.

A- Extended Hamming Product Code with type II HARQ

$P_{residual}$ depends on both the error detection capability in the first transmission and error correction capability after the retransmission. $P_{residual}$ is estimated as given in **Fu ,2009** as:

$$P_{residual} = P_{ud} + P(e_{decoding}, e_{detect}) \quad (2)$$

where P_{ud} is the undetectable error probability in the first transmission and $P(e_{decoding}, e_{detect})$ is the probability of error after retransmission and three stage decoding is over.

P_{ud} given in **Fu ,2009** as:

$$P_{ud} = 1 - (P_{ne} + P_c + P_d) \quad (3)$$

where P_{ne} is the probability of no error and P_c, P_d are the probability of correctable error patterns and the probability of detectable but uncorrectable error patterns in the first retransmission, respectively. $P(e_{decoding}, e_{detect})$ can be expressed as:

$$P(e_{decoding}, e_{detect}) = P_d \cdot (1 - P_{ne} - P_c) \quad (4)$$

By inserting (4) and (3) in (2) we get

$$P_{residual} = 1 - (1 + P_d) \cdot (P_{ne} + P_c) \quad (5)$$

Since any error pattern with at most one error in each row can be corrected in the first transmission, P_c for random errors can be given in **Fu,2009** as:

$$P_c = \sum_{t=1}^{k_2} \binom{k_2}{t} n_1^t \epsilon^t \quad (6)$$



where k_2 is the number of rows and n_1 is the row encoded word size. After retransmission, the proposed work can correct five random errors so P_d for random errors is defined in (7) as given in **Fu, 2009**. The first term is the error detection probability when two or three random errors occur in the first transmission. The second and third terms in (7) are the error detection probability of four and five random errors.

$$P_d = \sum_t^3 \binom{k_2}{1} \binom{n_1}{2} \binom{(k_2-1)n_1}{t-2} \epsilon^t + \left(\binom{k_2}{1} \binom{n_1}{2} \binom{(k_2-1)n_1}{2} \right) \epsilon^4 + \left(\binom{k_2}{1} \binom{n_1}{2} \binom{(k_2-1)n_1}{2} \right) \epsilon^5 \tag{7}$$

The probability of no error in the first transmission can be expressed as in **(Fu, 2009)**

$$P_{ne} = (1 - \epsilon)^{k_2 n_1} \tag{8}$$

By substituting (6), (7) and (8) in (5) $P_{residual}$ can be easily found.

B-MECCRLB

The multi-bit error correction scheme MECCRLB proposed in **Vinodhini and Murty, 2018** is an FEC-based coding scheme, where there is no retransmission available. As a result, $P_{residual}$ depends on the coding correction capability.

$$P_{residual} = 1 - (P_c + P_{ne}) \tag{9}$$

where

$$P_{ne} = (1 - \epsilon)^{k_2 \times n_1 + 10} \tag{10}$$

Vinodhini and Murty, 2018 indicated that MECCRLB can correct up to 11 random errors in 32-bit message so P_c for random errors was expressed as:

$$P_c = \binom{k_2 \times n_1 + 10}{12} \epsilon^{12} \tag{11}$$

However, the equation is not accurate as it is not possible to correct all the 11 random errors applying the MECCRLB decoding. The minimum Hamming distance d_{min} represents the minimum number of bits that can be changed between two different valid codewords. Based on this distance, the maximum correction and detection capability of any coding scheme can be given by $[(d_{min} - 1)/2]$. Applying this to MECCRLB code $d_{min} = (d_{min \text{ for extended hamming code}} \times d_{min \text{ simple parity check}})$ which equals to $d_{min} = (4 \times 2) = 8$, it can be inferred that the maximum correction capability for MECCRLB code is $[(8 - 1)/2]$ which equals to three errors. This represents the theoretical limit of this coding scheme assuming that the simple parities are calculated for all columns; which is not the case in



MECCRLB. **Fig .4** shows some cases where MECCRLB fails to correct two, three, and four errors. Instead, a new error correction model is derived in this work as given in equation (12) which expresses the correction capability for up to four random errors where the first term represents single error correction in a message shown in **Fig .4** (a). The second term expresses double errors correction in a message except if one of errors happens in 10-bits parity checks shown in **Fig .4** (b). Term three expresses the correction of three errors in a message except if one or two of the errors happen in 10-bits parity checks shown in **Fig .4** (c). Term four expresses the cases when MECCRLB succeeds to correct four errors in three cases; the first case is when all four errors are in one row, the second case is when three errors are in one row and the other are in any other message bits, and the third case is when two errors are in one row and the other two errors are elsewhere in the message as shown in **Fig .4** (d). However, there are also few cases where MECCRLB also succeeds to correct four errors but with negligible effect and adding them makes the equation more complex.

$$\begin{aligned}
P_C = & \binom{k_2 \times n_1 + 10}{1} \varepsilon + \left(\binom{k_2 \times n_1 + 10}{2} - \binom{k_2}{1} \binom{n_1}{1} \right) \varepsilon^2 \\
& + \left(\binom{k_2 \times n_1 + 10}{3} - \binom{k_2}{1} \binom{n_1}{2} 10 - \binom{k_2}{1} \binom{n_1}{1} 10 \right) \varepsilon^3 \\
& + \left(\binom{k_2}{1} \binom{n_1}{4} + \binom{k_2}{1} \binom{n_1}{3} \binom{k_2 \times n_1}{3} \right) \\
& + \left(\binom{k_2}{1} \binom{n_1}{2} \binom{(k_2 - 1) \times n_1}{2} \right) \varepsilon^4
\end{aligned} \tag{12}$$

If we substitute (12) and (10) in (9), $P_{residual}$ for MECCRLB for random errors can be found. After getting the equation for $P_{residual}$ for both Extended Hamming Product Code with type II HARQ and MECCRLB, for 32-bits message size the equations become a function of ε .



Figure 4. Examples of success and failure cases for work in **Vinodhini and Murty ,2018**
 (a)one-bit error in message (b)two-bit error in message(c)three-bit error in message(d)four-bit error in message.

4. RESULTS AND DISCUSSION

A testing program was written in (C++) to test the correction capability of the two schemes. **Table. I** shows the simulation results for both schemes, where 10^5 samples of 32-bit messages are fed to the two error correction schemes and some errors are injected. The failure percentage is found by:



$$Failure\ percentage = \frac{the\ number\ of\ uncorrected\ messages}{the\ total\ number\ of\ samples} \times 100\% \tag{13}$$

First, all samples are injected with one error randomly located in the message. It was noticed that both schemes can correct all combinations of one-bit error. Second, all samples are injected with two-bit errors randomly located in the message. HPC was able to correct all cases while MECCRLB failed to correct 32.5% of them. For three errors, HPC fails in 5.18% of the cases which is lower than the MECCRLB failure, namely 38.97%. Similarly, HPC showed lower failure percentage at 4 errors as compared with MECCRLB. We notice the huge diverge between HPC and MECCRLB correction capability.

Table .1 Simulation results.

Number of errors	HPC Failure Percentage	MECCRLB Failure Percentage
1	0%	0%
2	0%	32.5%
3	5.18%	38.97%
4	16.48%	69.8%

To validate the derived model, **Fig .5** shows $P_{residual}$ in estimation and simulation for 32-bit message size with different ϵ values. k_2 for HPC is four and three for MECCRLB. The two techniques were simulated using the (C++) program and random errors are injected at different positions and at different bit error rates for 10^8 codeword samples. Then, after applying the codewords to decoding algorithms for both schemes the simulation program will calculate the percentage of failure cases for each scheme which represents the simulated residual flit error rate. The results show that the estimated residual flit error rate is close to the simulated results which validates the correctness of the derived model. It can also be noticed by looking to the Y-axis that for the same values of $P_{residual}$ HPC sustains higher bit error rate which means it can achieve the same reliability level ($P_{residual}$) but at lower voltage swing which it is translated into lower power consumption. The relation between the bit error rate and the voltage swing is usually modeled using the Gaussian noise model as discussed in many works (**Fu,2009, Vinodhini and Murty, 2018**).

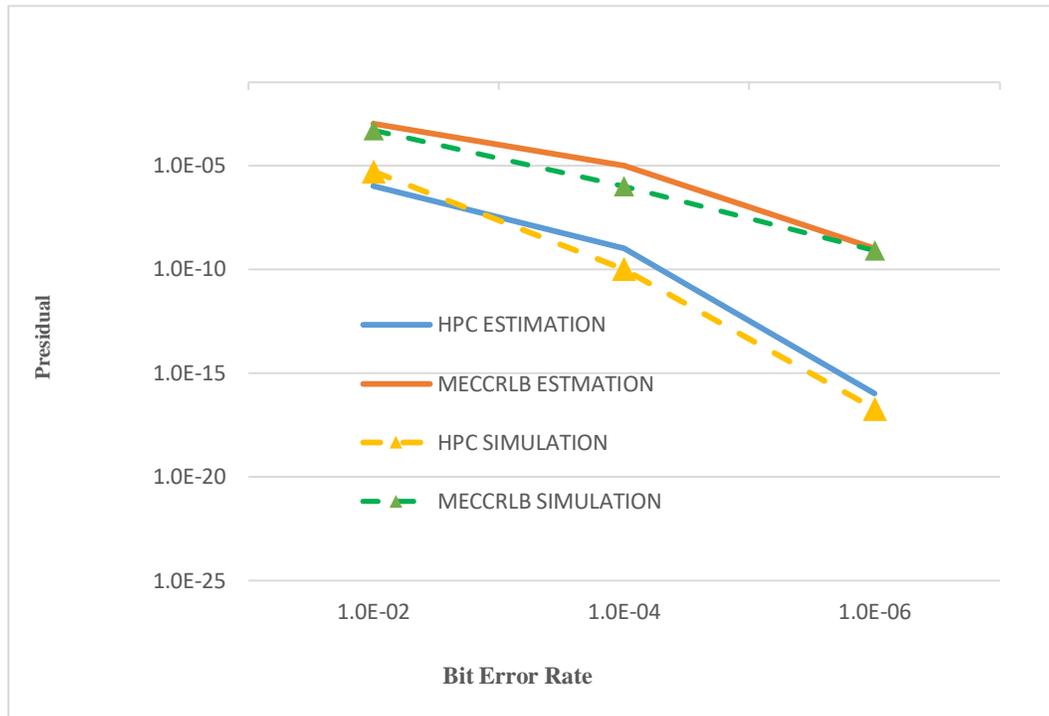


Figure 5. Residual for different Bit Error Rates.

5. CONCLUSIONS

In this paper, an accurate mathematical model to calculate the residual error probability P_{residual} for MECCRLB coding scheme was derived. The new estimation is highly correlated to the simulation results which prove the inaccuracy of old estimation results. The new results compared to Extended Hamming Product Code with type II HARQ showed that the latter has higher reliability due to its higher error correction capability, where HPC can correct all messages with two errors and very high percentage of messages that have three errors while MECCRLB code corrects only 68% of messages with two errors and 61% of messages with three errors.

Accordingly, it is expected that MECCRLB will have higher link voltage swing which is translated into higher power consumption. Thus, the schemes should be reanalyzed from power perspective using the accurate models. The HPC is still a promising coding scheme that can be used to address the reliability issues but requires some optimization at the encoder and decoder to reduce its complexity.

REFERENCES

- A. Ejlali, B. M. Al-Hashimi, P. Rosinger, and S. G. Miremadi, "Joint consideration of fault-tolerance, energy-efficiency and performance in on-chip networks," in Proc. Des., Autom. Test Eur. Conf. Exhib. (DATE 2007), Apr. , pp. 1–6.



- A. Ganguly, P. Pande, B. Belzer, “Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NOC Interconnects”, IEEE Trans. On very Large Scale Integr. (VLSI) Syst (2009) vol. 17, no. 11 1626-1639.
- A. K. Kummary, P. Dananjayan, K. Viswanath and V.Reddy “Combined Crosstalk Avoidance Code with Error Control Code for Detection and Correction of Random and Burst Errors “, June 12th 2019 intechopen.83561. Available from : <https://www.intechopen.com/online-first/combined-crosstalk-avoidance-code-with-error-control-code-for-detection-and-correction-of-random-and>
- A.Ganguly, A.P., Pande ,B., P., Belze r, B., “Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NOC Interconnects”, IEEE Transaction of VLSI Systems. Volume 17(11). pp. 1626 – 1639. Oct (2009).
- B .Fu and P. Ampadu, “A multi-wire error correction scheme for reliable and energy efficient SoC links using Hamming product codes”, in proc. IEEE Int. SOC conference (SOCC) (2008) 15-19.
- B.Fu and P .Ampadu, “Burst Error Detection Hybrid ARQ with crosstalk delay reduction for reliable on chip Interconnects”, IEEE Int. Symposium on Detect and fault tolerance in VLSI systems (2009) 440-448.
- B. Fu and P .Ampadu, “A multi-wire error correction scheme for reliable and energy efficient SoC links using Hamming product codes”, in proc. IEEE Int. SOC conference (SOCC) (2008) 15-19. on chip Interconnects using Hamming product codes, VLSI Des. (2008) 1-14.
- B .Fu and P. Ampadu, “On Hamming Product Codes with Type II Hybrid ARQ for On-chip Interconnects,” IEEE Trans on Circuits and Systems, vol. 56, no. 9, (2009) 2042-2054.
- B.Fu and P. Ampadu,” An Energy-Efficient Multi wire Error control scheme for Reliable on chip Interconnects using Hamming product codes”, VLSI Des. (2008) 1-14.
- C. Constantinescu, Trends and challenges in VLSI reliability IEEE Micro, vol. 23 no. 4, (2003) 14-19.
- D. Bertozzi, L. Benini, and G. De Micheli, “Error control schemes for on-chip communication links: The energy-reliability tradeoff,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., (2005) 24 . 818–831.
- M .Lajolo, M .Reorda and M. Violante, Early evaluation of bus interconnects dependability for system-on-chip designs, in Proc. of Int. Conf. VLSI Design (2001) 371-376.



- M. Gul, M. Chouikha, M.Wade, "Joint Crosstalk Aware Burst Error Fault Tolerance Mechanism for Reliable on-Chip Communication", IEEE Transactions on Emerging Topics in Computing (2017).
- M. Maheswari and G. Seetharaman, "Multi bit random and burst error correction code with crosstalk avoidance for reliable on chip interconnection links", Microprocessors and Microsystems, Volume 37, pp. 420-429,(2013).
- M. Vinodhini, N.S. Murty," Reliable low power NoC interconnect", Microprocessors and Microsystems 57(2018) 15-22
- N. Jafarzadeh, M. Palesi, S. Eskandari, S. Hessabi, A. Afzali-Kusha, Low energy yet reliable data communication scheme for Network-on-Chip, IEEE Trans. Comput. Aided-Des. Integr. Circuits Syst. 34 (12) (2015) 1892–1904.
- P.Narayanasmy,P ,S.and Muthurathinam ,S "Design of Crosstalk Prevention Coding scheme based on Quintuplicated Manchester error correction method for Reliable on chip Interconnects," Advances in Electrical and Computer Engineering ,vol 18,pp 113-130,(2018)
- S. Murali, T. Theocharides, N. Vijaykrishnan, M. J. Irwin, L. Benini, and G. De Micheli, "Analysis of error recovery schemes for net- works-on-chips," IEEE Des. Test Comput., vol. 22, pp. 434–442, Sep./Oct. (2005).
- S. Sridhara and N. R. Shanbhag, "Coding for system-on-chip networks: A unified framework," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, pp. 655–667, Jun. (2005).
- W.N. Flayyih, K. Samsudin, S.J. Hashim , Y. Ismail, F. Z.Rokhani. Multi-bit error control coding with limited correction for high-performance and energy-efficient network on chip. IET Circuits, Devices & Systems, vol 14 pp. 7 – 16., Jan (2020)
- W.N.Flayyih, W.N., K.Samsudin, S.J. Hashim, et al: 'Crosstalk-aware multiple error detection scheme based on two-dimensional parities for energy-efficient network on chip', IEEE Trans. Circuits Syst. I, Regul.Pap., (2014), 61, (7), pp. 2034–2047

NOMENCLATURE

VDSM=very deep-*submicron*.

$P_{residual}$ = probability of residual error.

P_{ne} = the probability of no error.

d_{min} = minimum hamming distance.