Development of an On-Line Self-Tuning FPGA-PID-PWM Control Algorithm Design for DC-DC Buck Converter in Mobile Applications

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ABSTRACT

This paper presents a new development of an on-line hybrid self-tuning control algorithm of the Field Programmable Gate Array - Proportional Integral Derivative - Pulse Width Modulation (FPGA-PID-PWM) controller for DC-DC buck converter which is used in battery operation of mobile applications. The main goal in this work is to propose structure of the hybrid Bees-PSO tuning control algorithm which has a capability of quickly and precisely searching in the global regions in order to obtain optimal gain parameters for the proposed controller to generate the best voltage control action to achieve the desired performance of the Buck converter output. Matlab simulation results and Xilinx development tool Integrated Software Environment (ISE) experimental work show the robustness and effectiveness of the proposed on-line hybrid Bees-PSO tuning control algorithm in terms of obtaining smooth and unsaturated state voltage control action and minimizing the tracking voltage error of the Buck converter output. Moreover, the fitness evaluation number is reduced.

Keywords: Buck Converter; Digital PID Controller; On-Line; Self-Tuning; Bees-PSO Algorithm; FPGA.

تطوير لتصميم خوارزمية سيطرة (مصفوفة البوابات المنطقية القابلة للبرمجة – التناسبي التكاملي التفاضلي - تعديل عرض النبضة) تلقائية التنغيم وبشكل حي متصل لمحول خفض التيار المستمر في التطبيقات النقالة

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الخلاصة

يقدم هذا البحث تطوير جديد لخوارزمية تنغيم المسيطر بصورة تلقائية وبشكل حي متصل لمسيطر(مصفوفة البوابات المنطقية القابلة للبرمجة – التناسبي التكاملي التفاضلي - تعديل عرض النبضة) للمحول الخفض للتيار المستمر الذي يستخدم في عمل البطارية للتطبيقات النقالة .إن الهدف الرئيسي من هذا العمل هو اقتراح هيكلية لخوارزمية الهجينة (النحل – أمثلية حشد الجسيمات) لتنغيم المسيطر والتي لها القابلية على البحث السريع و المضبوط في المناطق العالمية لكي يحصل على امثل عناصر الكسب للمسيطر المقترح لتوليد أفضل فولتية فعل سيطرة لتحقيق الأداء المطلوب للخراج المحول الخفض .
أن نتائج المحاكاة (الحقيبة البرمجة ماتلاب) والعمل التجريبي (الحقيبة البرمجية زيلينكس) اثبت متانة وفعالية للخوارزمية الهجينة المقترحة من حيث الحصول على فعل سيطرة ناعم بدون حالة الإشباع وتقليل تتابع الخطأ لفولطية الإخراج للمحول الخفض. وبالإضافة إلى تقليل عدد استدعاء لدالة التقييم.

الكلمات الرئيسية: محول خافض، مسيطر رقمي ، بشكل حي ومتصل، تنغيم ذاتي، خوارزمية النحل-حشد الجسميات.

1. INTRODUCTION

In the last decade, the mobile applications in our life have been increased such as mobile phones and laptops. Thus, the design and the control of DC-DC converter power switching circuits for battery operation are required in order to achieve voltage regulation with fast transient response and high conversion efficiency, **Chander, et al., 2013** and **Emami, et al., 2008.**

Therefore, there are different types of control algorithms for the Buck converter. These algorithms are based on the mathematical model of the power switching circuit of the DC-DC converter and they are proposed to achieve the desired output voltage with variable load current and fast dynamic response as well as high efficiency with high performance of the controllers, such as PI controller, **Garg, et al. 2015,** fuzzy logic and PID controllers, **Tapou, et al. 2011,** adaptive hysteresis controllers, **Kim, et al. 2012** and **Chuang, et al. 2011**, pole placement controller **Kelly,** and **Rinne, 2005**, state feedback controller **Keller, et al. 2005**, LQR method controller, **Leung, et al. 1993**, sliding model controller, **He,** and **Luo, 2004,** and switching control with time delay controller based FPGA, **Themozhi,** and **Reddy, 2014**.

The motivation of this work is to handle Buck converter dynamic behaviors problems, which affect the work of the portable devices. These problems are summarized by: variable output voltages; wide range of loading current and various input voltage levels. In order to solve these problems in the transient and steady-state responses in the closed loop system, the on-line hybrid Bees-PSO tuning algorithm of adaptive PID controller based FPGA is proposed in this paper. This tuning control algorithm is a modified version of the Bees algorithm.

The contributions of this work is described as follows:

- Proposing of the hybrid Bees-PSO control algorithm which has the ability of the fast on-line searching in global regions to get and tune the best gain parameters for the adaptive PID controller. These parameters are responsible of generating the best voltage control action. Thus, the output voltage of the Buck converter will quickly reach the desired output voltage in the transient response.
- Verifying the PID controller adaptation performance by changing the input voltage levels of the Buck converter .
- Investigating the performance of the adaptive PID controller robustness by adding a load disturbance.
- Verifying the design and the implementation of the on-line digital PID controller with the pulse width modulation by using FPGA-Xilinx-Virtex-5 xc5vlx5 board for the Buck converter system
- Validating experimentally the proposed FPGA-PID-PWM controller as an embedded integrated circuit.

The Matlab simulation results of adaptive PID controller and the Xilinx Virtex-5 board experimental work for the FPGA-PID-PWM controller show preciously the same performance for the Buck converter model in terms of minimizing the voltage error and in generating the best voltage control action.

The organization of this paper can be described as follows: Section two, contains the Buck converter circuit mathematical model. Section three, describes the proposed design structure of FPGA-PID controller. Section four, demonstrates the proposed hybrid Bees-PSO tuning control algorithm. Section five, considers the performance of the adaptive PID controller through simulation results. Section six, shows the design and the verification of the FPGA-PID-PWM

controller based on Xilinx Virtex-5 xc5vlx50 board and Xilinx ISE 14.5 respectively as experimental work. Finally, section seven gives the conclusions from this paper.

2. BUCK CONVERTER CIRCUIT MODEL

In general, the Buck converter belongs to the class of Chopper circuits, or attenuation circuits. It actually multiplies the constant input source voltage V_{Supply} by a scalar factor, smaller than unity, then the output voltage V_{out} of Buck converter is less than the input source voltage V_{Supply}, **Chander, et al., 2013**.

Fig. 1, shows the simplified schematic of the synchronous Buck power stage which has controllable n-channel MOSFETs power switches, **Chander, et al., 2013** and **Tapou, et al. 2011** to achieve the operation condition. The figure indicates Q_1 is the MOS switch and Q_2 is the MOS synchronous rectifier which replaces the diode rectifier in order to increase the circuit efficiency, V_{Supply} is the source voltage, V_{out} is the output voltage, L is the converter main inductance, C is the main capacitor and R_{Load} is the load resistance, the on channel resistance of the switch and synchronous rectifier MOS transistors (rs_{on}), the effective series resistance of the inductor (r_L) and capacitor (r_C).

To analyze the operation of the circuit and describe the mathematical model, there are two time of operation (Ton) and (Toff) which depend on two MOSFET (Q1 and Q2) as follows:

Switching ON Q1 and switching OFF Q2:

At a period of time t<T1, the circuit analysis can be described by applying Kirshoff's voltage law as follows:

$$V_S - i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_{OUT} = 0 \quad (1)$$

Switching OFF Q1 and swithing ON Q2:

At a period of time T1<t<T2, the circuit analysis can be described by applying Kirshoff's voltage law as follows:

$$-i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_{OUT} = 0 \quad (2)$$

By defining Δ as a switching function as Eq. (3) to turn V_{Supply} ON and OFF

$$\Delta = \begin{cases} 1 & 0 < t < T_1 \\ 0 & T_1 < t < T_2 \end{cases} \quad (3)$$

Then Eq. (1) and Eq. (2) can be written as follows

$$\Delta V_S - i_L \cdot rs_{on} - L\frac{di_L}{dt} - i_L \cdot r_L - V_{OUT} = 0 \quad (4)$$

then

$$\frac{di_L}{dt} = \frac{1}{L}\left[(\Delta V_S - V_{OUT}) - i_L \cdot (rs_{on} + r_L)\right] \quad (5)$$

The output voltage of the Buck converter circuit V_{out} is written as:

$$V_{OUT} = i_L \cdot X_{Load} \quad (6)$$

where X_{Load} is the output impedance as in Eq. (7)

$$X_{Load} = \frac{R_L \times X_C}{R_L + X_C} \quad (7)$$

where

$$X_C = \frac{1}{SC} + r_C \quad (8)$$

Then, it can be written as:

$$X_{Load} = \frac{SCR_L r_C + R_L}{SC(R_L + r_C) + 1} \tag{9}$$

Substituting Eq. (9) into Eq. (6) results in:

$$SC(R_L + r_C)V_{OUT} = i_L(SCR_L r_C + R_L) \tag{10}$$

By taking the time derivative of both side for Eq. (10) we get

$$\frac{dV_{OUT}}{dt} = \frac{\frac{di_L}{dt}(CR_L + r_C) + i_L R_L}{C(R_L + r_C)} \tag{11}$$

Finally, substituting Eq. (5) in Eq. (11) gives

$$\frac{dV_{OUT}}{dt} = \frac{\frac{1}{L}[(\Delta V_S - V_{OUT}) - i_L \cdot (rs_{on} + r_L)](CR_L + r_C) + i_L R_L}{C(R_L + r_C)} \tag{12}$$

3. ADAPTIVE DIGITAL PID CONTROLLER DESIGN

Generally, PID controllers are widely used in industrial applications because of their simple structure which consists of three terms: proportional, integral and derivative **Emami, et al., 2008** and **Garg, et al. 2015**. The proposed on- line self-tuning adaptive PID controller structure in this paper is shown in **Fig. 2,** which has a strong adaptation performance, high dynamic characteristic and good robustness performance because of its ability in finding and tuning the PID control parameters.

The control action of the proposed on-line self-tuning adaptive PID controller is necessary to stabilize the error voltage of the Buck converter output when the output voltage drifts from the reference voltage and to give a good performance evaluation for uncertain parameters and for disturbance rejection.

The PID controller time-domain form is given by Eq. (13), **Garg, et al. 2015**:

$$u(t) = k_p e(t) + k_i \int_0^t e(t)d(t) + k_d \frac{de(t)}{dt} \tag{13}$$

where k_p is the proportional gain; k_i is the integral gain; k_d is the derivative gain; *u(t)* is the control action and *e(t)* is the error signal.

In order to implement the adaptive PID controller in FPGA, the continuous controller of Eq. (13) is simply replaced by a digital equivalent one using the z-transform where the integration and differentiation are performed numerically .The trapezoidal rule for numerical integration, and the backward difference for numerical differentiation, will be used as a common method for transformation, **Sravanthi,** and **Rajkumar, 2014** thus, Eq. (14) will represent the digital form for Eq. (13)

$$U(Z) = [k_p + \frac{k_i T_s}{2}\frac{1 + Z^{-1}}{1 - Z^{-1}} + k_d \frac{1 - Z^{-1}}{T_s}]E(Z) \tag{14}$$

where T_S : The sampling time.

In a discrete time at k^{th} samples, the actual output of the controller *u(k)* can be represented as follows:

$$u(k) = k_p e(k) + F(k) + \frac{k_d}{T_s}(e(k) - e(k-1)) \tag{15}$$

$$F(k) = F(k-1) + \frac{k_i T_s}{2}(e(k) + e(k-1)) \quad (16)$$

The structure of the digital PID controller will be realized, as shown in **Fig. 3,** based on Eq. (14). Obviously, it is composed of three multiplications and five accumulations operations. **Fig. 4,** demonstrates the FPGA–PID block diagram for **Fig. 3**.

4. HYBRID (BEES-PSO) TUNING ALGORITHM

The proposed hybrid Bees-PSO tuning algorithm is created by mixing two search algorithms. The first one is the Bees algorithm which mimics of the food foraging behavior of swarms in honey bees. This algorithm is carried out by using two searches the neighborhood search that has two types of Bees (Selected and Recruit Bees) and the global (random) search that has also two types of Bess (Scout and Fittest Bees), **Pham, et al., 2005** and **Pham, et al., 2006**.

The second algorithm is Particle Swarm Optimization PSO which has the capability to search for the optimal solution by simulating the movement and flocking of birds. Particles represent population of individual search one which has its position and velocity to move around the search space till finding the best or optimal solution by using the fitness function, **Wang, et al. 2017**.

The hybridization comprises the use of the PSO algorithm to generate the population (Recruit Bees) as particles in the neighborhood search region of the Bees algorithm then combining the (Fittest Bees from PSO algorithm) with the new (Scout Bees) to generate the new population in the global search area of the Bees algorithm. This mixing improves and speeds up the optimization process significantly.

The proposed hybrid algorithm is used to find and tune the optimal gains control for the adaptive PID controller to generate the best and the smooth voltage signal that leads to minimize the Buck converter output voltage error during variable load.

The flowchart diagram of the proposed hybrid Bees-PSO tuning control algorithm is shown in **Fig. 5**.

In this work, the Scout-Bees (n) are generated as the initial population with random three values of the PID controller's parameters and it is used the fitness Eq. (17), **Al-Araji, 2014,** based cost function.

$$fitness = \frac{1}{\mu + Cost\ Function} \quad (17)$$

where: $\mu > 0$ to avoid division by zero.

The cost function is a mean square error as in Eq. (18) .

$$MSE = \frac{1}{N}\sum_{i=1}^{N}[(V_{ref} - V_{OUT})^2 \quad (18)$$

N: is the number of iterations.

The size of (patch size) the neighborhood search (Selected-Bees (m)) is determined by applying the proposed Eqs. (19,20,21).

$$\Delta Kp = 0.5 \times Kp_{old} \times random(0,1) \quad (19)$$

$$\Delta Ki = 0.1 \times Ki_{old} \times random(0,1) \quad (20)$$

$$\Delta Kd = 0.2 \times Kd_{old} \times random(0,1) \quad (21)$$

Then, the particles (Recruit-Bees) are generated by using Eqs. (22, 23, 24) in order to search and find the best controller's parameters.

$$Kp_{new} = Kp_{old} + \Delta Kp \quad (22)$$

$$Ki_{new} = Ki_{old} + \Delta Ki \quad (23)$$

$$Kd_{new} = Kd_{old} + \Delta Kd \quad (24)$$

Then, each best particle (Fittest-Bees) depends on the Eqs. (17,18) is updated by using Eqs. (25 - 30).

$$\Delta Kp_m^{k+1} = \Omega \Delta Kp_m^k + c_1 r_1 (pbest_m^k - Kp_m^k) + c_2 r_2 (gbest^k - Kp_m^k) \quad (25)$$

$$Kp_m^{k+1} = Kp_m^k + \Delta Kp_m^{k+1} \quad (26)$$

$$\Delta Ki_m^{k+1} = \Omega \Delta Ki_m^k + c_1 r_1 (pbest_m^k - Ki_m^k) + c_2 r_2 (gbest^k - Ki_m^k) \quad (27)$$

$$Ki_m^{k+1} = Ki_m^k + \Delta Ki_m^{k+1} \quad (28)$$

$$\Delta Kd_m^{k+1} = \Omega \Delta Kd_m^k + c_1 r_1 (pbest_m^k - Kd_m^k) + c_2 r_2 (gbest^k - Kd_m^k) \quad (29)$$

$$Kd_m^{k+1} = Kd_m^k + \Delta Kd_m^{k+1} \quad (30)$$

where: $m = 1,2,3,.....pop$; $Kpid_m^k$ are the particle's weight m at k^{th} iteration; Ω : is the inertia weight factor is equal to 0.79; c_1 and c_2 are the positive values; r_1 and r_2 are random numbers between 0 and 1; P_{bestm} is best previous weight of m^{th} ; Particle and g_{best} is best particle among all the particle in the population.

The hybrid Bees-PSO algorithm for finding and tuning control parameters is repeated at 4μsecond (sampling time) for each k^{th} sample based on Shannon theorem.

5. MATLAB SIMULATION RESULTS

The Buck converter power circuit specifications are taken from, **Garg, et al. 2015** and **Tapou, et al. 2011**, as shown in **Table 1**. The MATLAB simulation is carried out on-line hybrid Bees-PSO tuning control algorithm with adaptive PID controller, as shown in **Fig. 2**, to follow the desired output voltage for the DC-DC Buck converter with sampling time equal to 4μsec based on the time constant of the model τ=26μsec that depends on the damping ratio ζ= 1.1023 and the natural frequency wn=$3.4703\times10^{+4}$ rad/sec of the Buck converter model. Therefore, the dynamic behaviour of the Buck convert output is fast, hence it needs to a fast self-tuning control algorithm to generate the control action.

In this paper, to show that the adaptive PID controller with hybrid Bees-PSO tuning control parameters has a capability of fast generating optimal and smooth voltage control action and minimizing the voltage error with minimum number of iterations, the parameters of the optimization hybrid Bees-PSO algorithm will be defined as shown in **Table 2.**

The simulation results of the variable step change in the desired output voltage of the Buck converter based closed loop voltage control system with on-line tuning adaptive PID controller with initial output voltage of zero volt can be shown in **Figs. 6-a, b, c**, so the response of the output voltage of the Buck converter model to variable step changes as (2.25, 1.75 and 1.25) volt was very small over shoot at 0.2 msec and zero steady-state error in each step change, as shown in **Fig. 6-a**.

The voltage error between the desired output voltage and the actual output voltage of the Buck converter model was small value in the transient at each step change of the desired value and became zero value at steady state, as shown in **Fig. 6-b**.

Fig. 6-c, shows the adaptive PID control action response which has very small spikes in response to the first desired voltage step change (2.25 volt) without oscillation. The control action did not reach the saturation state action where the maximum value of the control action is 3.75 volt based on the battery supply voltage.

In this work, Mean Square Error (MSE) for on-line hybrid Bees-PSO tuning control algorithm has clearly improved the performance of the adaptive PID controller by showing the voltage error convergence for the Buck converter model at 300 samples, as shown in **Fig. 7**.
To investigate the on-line tuning control algorithm based hybrid Bees-PSO is better than other algorithms in terms of the effects of iteration number. In the local search, the iteration number is equal to 3 while in the global search it is equal to 4 via summing all the values of on-line mean square error, as shown in **Fig. 8**.
The parameters of the adaptive PID controller *kp, ki* and *kd* that have been tuned on-line based on hybrid Bees-PSO algorithm at each sample are shown in **Figs. 9-a, b, c,** respectively.
The response of the output voltage of the Buck converter model to a step change (1.25) volt with variable load resistance that decreases by 10% at 0.225 msec as adding a disturbance, in order to verify the robustness performance of the adaptive PID controller. It had small over shoot at 0.275 msec with very small oscillation during adding disturbance but at steady-state, the error was equal to zero value as shown in **Fig.10-a**.
Fig. 10-b, shows the error between the desired voltage and the Buck converter output voltage. The error has a small value at transient state and in steady state, the error became very close to zero with very small oscillation. **Fig. 10-c**, shows the control action which has a capability to track the voltage error of the Buck converter output to follow the desired voltage step change and reduce the effect of the load resistance disturbance as well as the model uncertainties on the system because of the strong adaptability and high robustness performance of the proposed controller trained by the powerful on-line hybrid Bees-PSO tuning control algorithm.

6. EXPERIMENTAL WORK

This section demonstrates in detail the design, implementation, verification and validation by device programming of the digital FPGA-PID-PWM using the Xilinx development tool Integrated Software Environment (ISE) version 14.5.
The simulation of all modules is done by using Verilog language and finally the experimental results are verified with Matlab simulation results. The schematic design methodology is used to make all modules of the controller which consists of three parts, the first part is digital PID that is based on two **Figs. 3, 4** and the second part is the digital pulse width modulation circuit and the third part is the digital control unit which controls and synchronizes the data flow of FPGA-PID-PWM. The most important issues in any digital design are to decide the finite word length, which restricts the real number representation of signals, variables and coefficients of constant number of bits also, it is very important to decide the type of arithmetic (fixed point or floating point) these two required decisions have obvious predication for the system dynamic response.
In this work, Matlab simulation is used to predict the following data: the voltage error signal values, control gains (kp, ki and kd) and control action values during 300 samples and according to the estimated signed data (1) decimal place is needed to represent the integer part and (3) decimal places are essentially to represent the fractional part thus, the economical 16 -signed fixed point arithmetic are used to get a high precision representation with the following details: 1 bit for sign which represents the most significant bit MSB, 4 bit for integer and finally 11 bit to represent the three decimal places of the fractional part and this is according to Eq. (31), **Ifeachor, et al., 2002,** and **Williamson, 1991**.

$$B \cong 3.3D \quad (31)$$

where D is number of decimal places; B is number of binary bits.

As mentioned above we have a signed data, thus two's complement arithmetic module, as shown in **Fig. 11-a**, is very essential to deal with signed number of the voltage error signal (input to the FPGA-PID-PWM). In digital design the two's complement format is preferred for arithmetic operations because it has only one representation for zero and moreover, the dynamic range is greater by one as compared with ons's complements and signed magnitude representation since one more number can be represented. Finally, its "not to overflow" which means that any intermediate overflow that may occur in reaching the end result is of no consequence.

The FPGA design for the two's complement module needs the following components as shown in **Table 3**. **Fig. 11-b**, shows the test bench waveform of the 2's complement arithmetic digital circuit using Verilog language. To obtain the output from this circuit two clocks and two control signals (Load_E and CO_E) are needed. The circuit detects the MSB which refers to the sign of the input voltage error signal number if it is equal to logic 0 this means a positive number and it will stay in its natural binary form if it is equal to logic 1 this means a detection for the negative number occurred then the complement of all binary bits will be taken and logic 1 is added to the LSB.

The schematic design sheet of the digital PID controller based on **Fig. 4**, is achieved and it required the following ICs Registers, Adders -Subtracts and Multipliers, as shown in **Fig. 12-a**. The Verilog language is used to simulate the design and test the operation of the digital PID, as shown in **Fig. 12-b**. The implementation of the digital PID needs component as shown in **Table 4**. The synchronization and the control of the data flow within the FPGA digital PID controller needs (11) eleven control signal, as shown in **Table 5**.

It is very important to explain that there is a need to add 2'S complement digital circuit with two control signals (Load_U and CO_U) before and after the PID controller module in order to detect negative and positive sing and convert the number if negative to the 2'S complement format thus, the over-all control signal will be fifteen signals. The data flow from the input (voltage error) to the output (control action) needs fifteen clocks, two clocks to get input 2'S complement, eleven clocks to get PID output and two clocks to get the 2'S complement of the control action which will be fed to the PWM circuit.

The digital Pulse Width Modulation (PWM) is digital circuit that gives a train of variable width pulses with fixed frequency and magnitude, **Angulo, et al., 2006.**

In this work, it is designed to convert the output "control action" of the digital PID controller to variable width pulses that is used as a gate control signals or the MOSFET power transistors (Q1 and Q2) to turn them to ON and OFF state.

The FPGA-PWM design needs the following IC: 8-bit comparator and 8-bit counter with one enable control signal. The control signal of the digital PID is normalized from 16 bit to 8 bit by truncation and this signal is fed to the first input of the comparator while the comparator's second input is fed by the eight bits counter which counts the 256 levels of the modulation control signal. The maximum PWM frequency is 265 kHz and the synchronization clock period of the system is 14.5 nsec. When the counter start counting, its value will be compared continuously with the normalized control signal and if the control signal is larger, the PWM output is set to one, otherwise, it is set to zero thus, the train of variable width will be created.

The synchronization and control of the FPGA-PID-PWM operation requires the design of a control unit that will achieve a sequence of pulses by using 16 bits Shift-Register with some Logic gates circuit to generate the 16 control pulses, as shown in **Fig. 13-a**.

The schematic design of the digital control and PWM digital circuit simulated using Verilog language to test the operation of the design is as shown in **Fig. 13-b**.

The FPGA-PWM and control unit design needs components as shown in **Table 6.** The overall schematic design of FPGA-PID-PWM controller is shown in **Fig. 14-a**, it needs components as shown in **Table 7**. **Fig. 14-b**, shows the top level design of FPGA-PID-PWM IC with its pins and controls.

To verify FPGA-PID-PWM in the Xilinx development tool (ISE Ver. 14.5) using Verilog language the following input data: voltage error signal and control parameters (kp, ki, kd) are fed continuously at each sample (272 clock) in form of a data files to the test bench to obtain the digital PWM control action, as shown in **Fig. 15**, and the output result is saved in another file.

Finally, to validate the output response of the digital FPGA-PID-PWM, it will be compared with the output response of the adaptive PID controller response, as shown in **Fig. 16**, and it is clear that the output voltage response of the Buck converter that is based on the digital FPGA-PID-PWM controller is approximately matching with the output voltage response of the Buck converter that is based on the adaptive PID controller because of many considerations that have been taken in the design of digital controller such as:

- Using 16 bits high precision representation for word length that led to no needed for scaling factor processing.
- Using two's complement that prevented the consequence of over flow.
- Fixed point fraction that overcame the over flow in multiplication point.

The maximum difference voltage in the Buck converter output between using two controllers in **Fig. 16**, did not access ±0.15 volt, as shown in **Fig. 17.**

Therefore, the implementation of FPGA-PID-PWM is downloaded to Xilinx Virtex5 xc5vlx50 board, as shown in **Fig. 18**, and this is done after generating the bit-stream file that successfully has been obtained from Xilinx-ISE (synthesize-XST, Implement Design and Generate Programming File) development system in order to validate the FPGA-PID-PWM controller as embedded integrated circuit.

7. CONCLUSIONS

The Matlab simulation results and Xilinx development tool Integrated Software Environment (ISE) experimental work on the on-line Bees-PSO tuning control algorithm of adaptive PID controller are based on FPGA presented in this paper for DC-DC Buck converter system. The proposed on-line tuning control gain parameters algorithm was responsible for the following:

- Fast pick up of the optimal control gain parameters with minimum number of fitness evaluation.
- Efficiency of obtaining the best voltage control action with no saturation state leads to save the energy of the battery supply.
- Effective minimization capability of tracking voltage error to track the reference voltage.
- Giving high robustness performance in reducing the variable load current effects.
- Making high performance output of FPGA-PID-PWM controller as embedded integrated circuit in terms of minimum number of control unit output signals and quickly and precisely generating control action.

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Table 1. The parameter values of the Buck converter model [3,4].

Description	Symbol	Value	Unit
The Converter Main Inductance	L	33	µH
The Main Capacitor	C	47	µF
The Load Resistance	R_{Load}	2.345	Ω
The Effective Series Resistance of The Inductor	r_L	66	mΩ
The Effective Series Resistance of The Capacitor	r_C	70	mΩ
The ON Channel Resistance of The Switch and Synchronous Rectifier MOS Transistors	rs_{on}	2.1	Ω
Supply Voltage	V_{Supply}	3.75	V

Table 2. The parameter values of the proposed tuning algorithm.

Scout Bees (n) is equal to 10 at the global search
The Selected Bees is equal to 5
The particle is equal to 20 in the neighborhood search;
The Fittest Bees is equal to 5
The iteration number (*N*) in the global search is equal to 4
The iteration number (*P*) in the neighborhood search is equal to 3.

Table 3. The two's complement module needs components.

LUTs slice	logic gates	occupied slices	LUT flip-flop pairs	flip-flop	bonded IOBs
81	82	41	82	16	35

Table 4. The digital PID module needs components.

LUTs slice	logic gates	occupied slices	LUT flip-flop pairs	flip-flop	bonded IOBs
272	281	140	281	144	91

Table 5. The control signals

No.	Signal Name	Signal operation
1	Clear	To clear all registers
2	CS1	To load the values of Kp, Ki, Kd
3	CS2	To operate the digital PID controller
4	CS3	
5	CS4	
6	CS5	
7	CS6	
8	CS7	
9	CS8	
10	CS9	
11	CS10	To load the data (digital control action) in the register

Table 6. The control unit with PWM module needs components.

LUTs slice	logic gates	occupied slices	LUT flip-flop pairs	flip-flop	bonded IOBs
40	42	35	45	25	43

Table 7. The FPGA-PID-PWM module needs components.

LUTs slice	logic gates	occupied slices	LUT flip-flop pairs	flip-flop	bonded IOBs
474	487	257	490	201	67

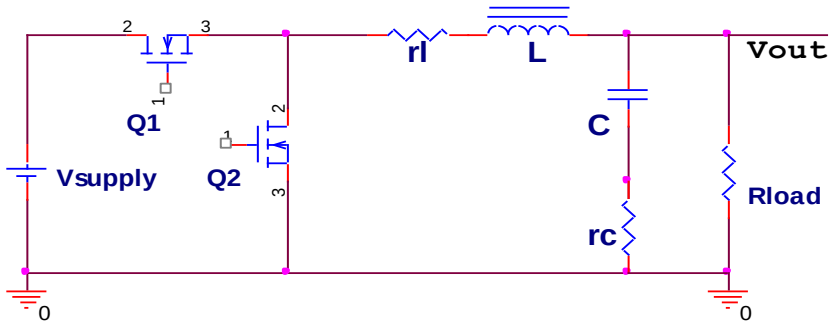


Figure 1. Synchronous Buck power stage schematic.

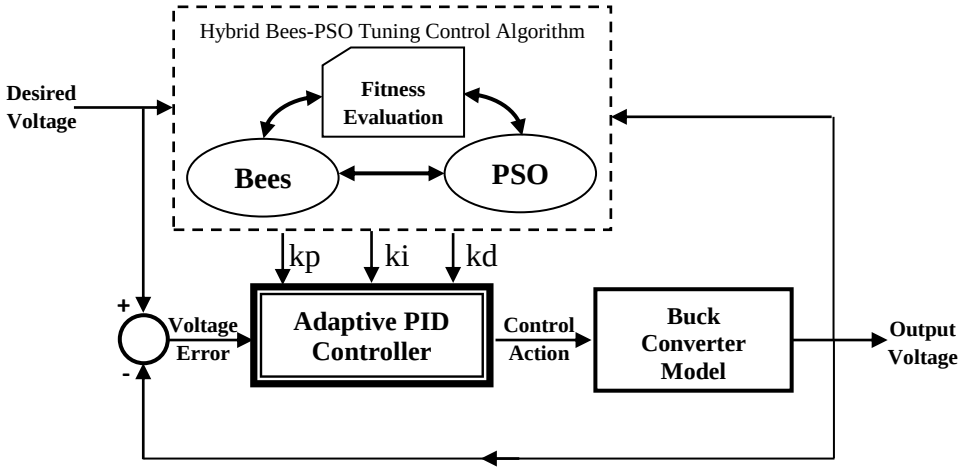


Figure 2. The block diagram of the adaptive PID controller for Buck converter model.

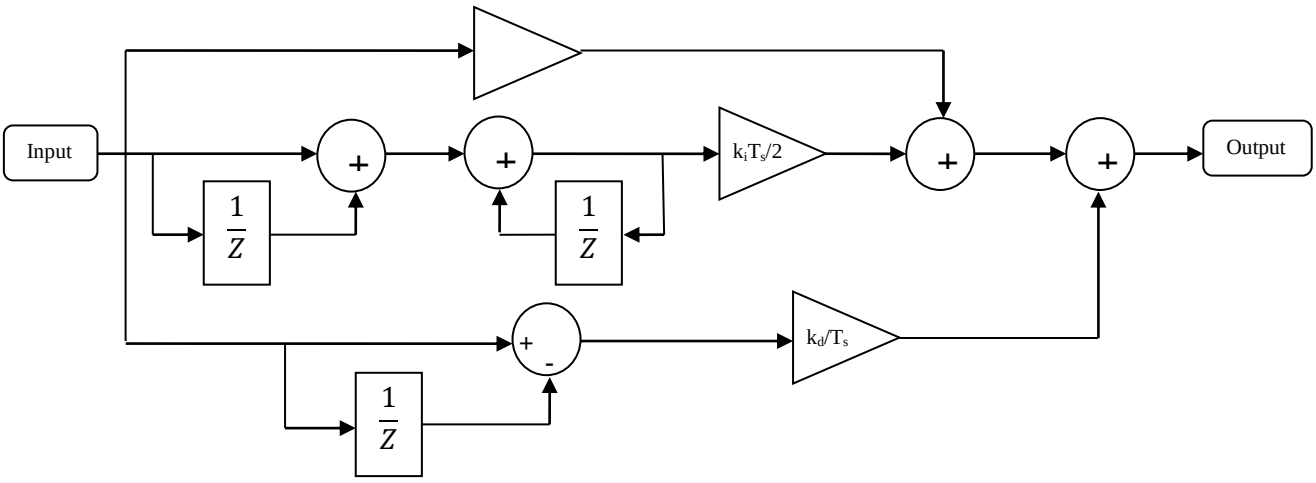


Figure 3. Digital PID controller realization.

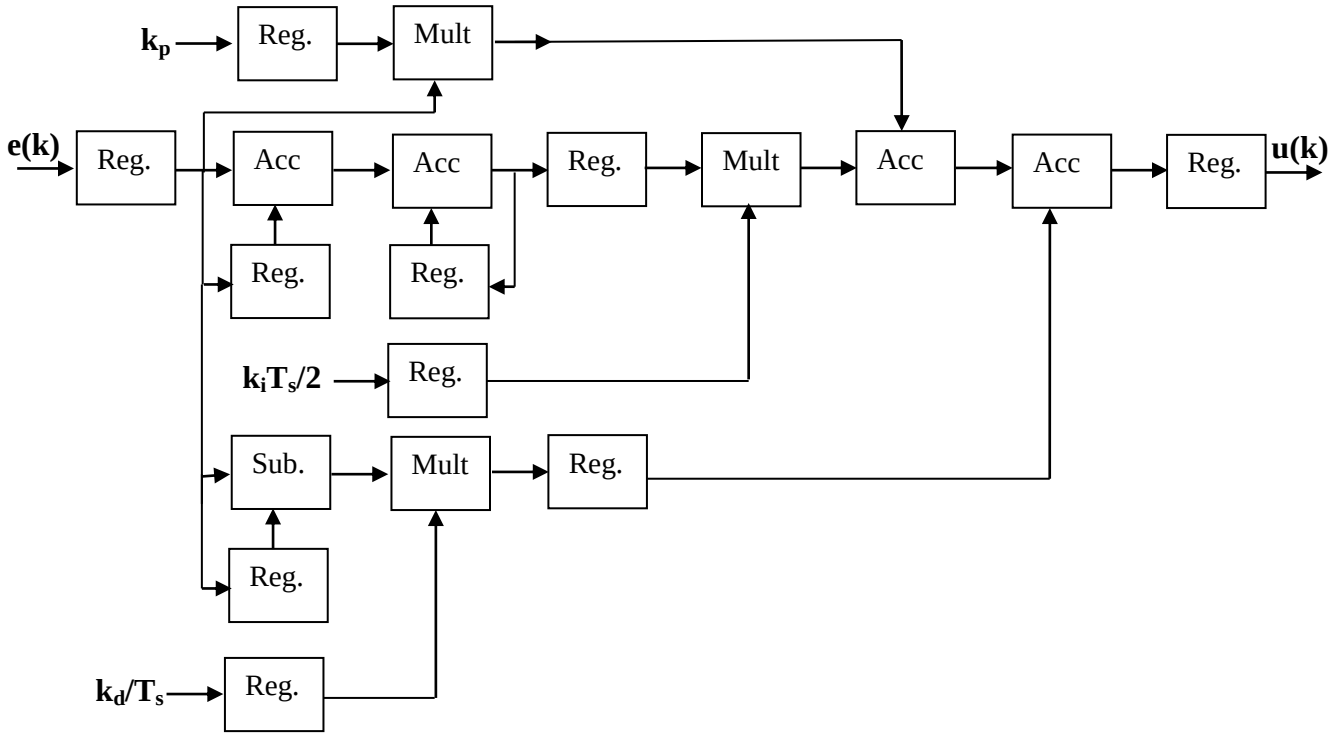


Figure 4. Block diagram of PID controller in FPGA.

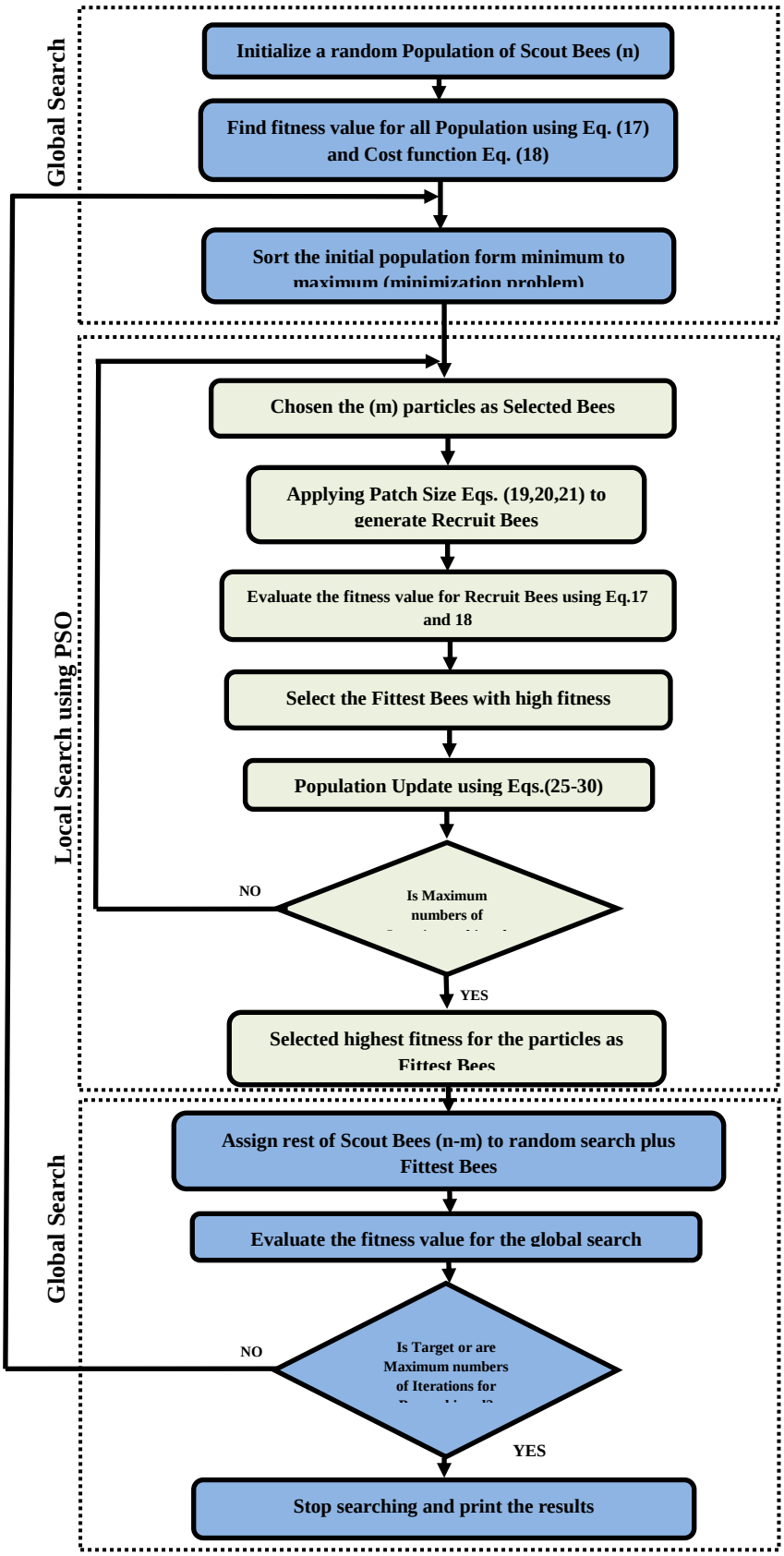


Figure 5. The proposed flow chart of the Bees-PSO algorithm.

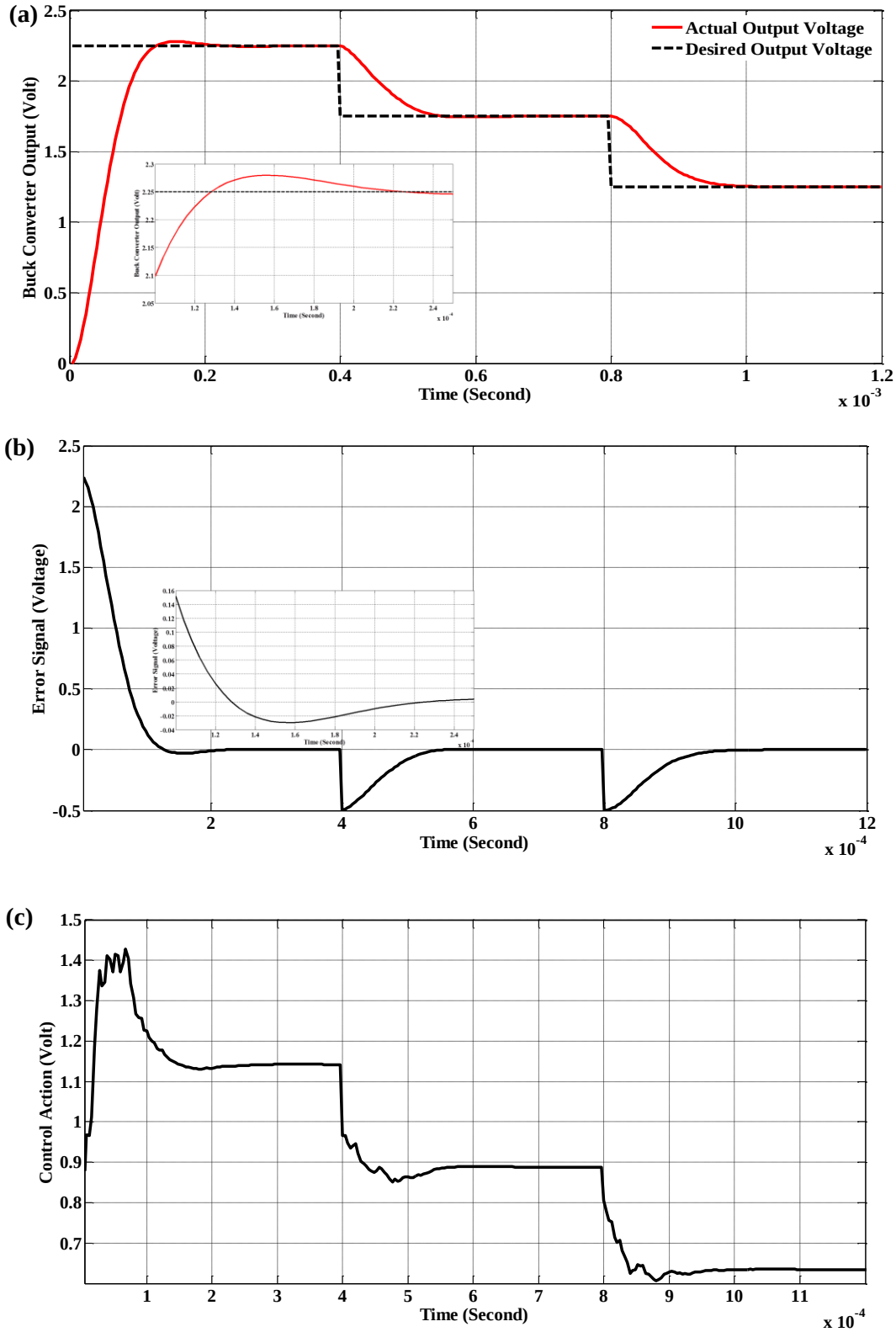


Figure 6. Simulation results of the adaptive PID controller (a) Output voltage for Buck converter model; (b) Voltage error; (c) Voltage control action.

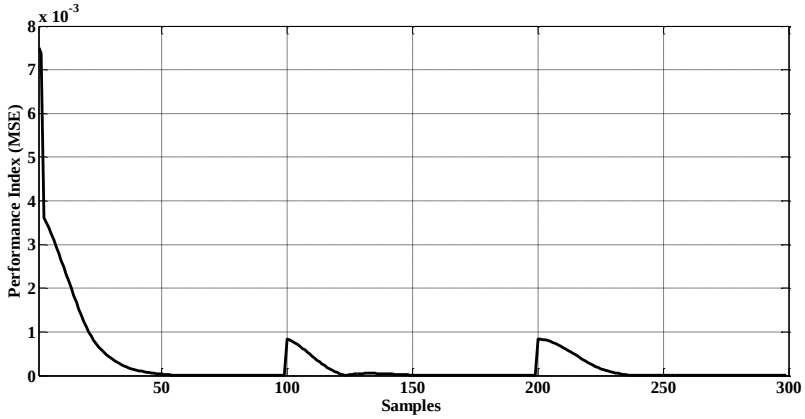


Figure 7. On-line performance index (MSE).

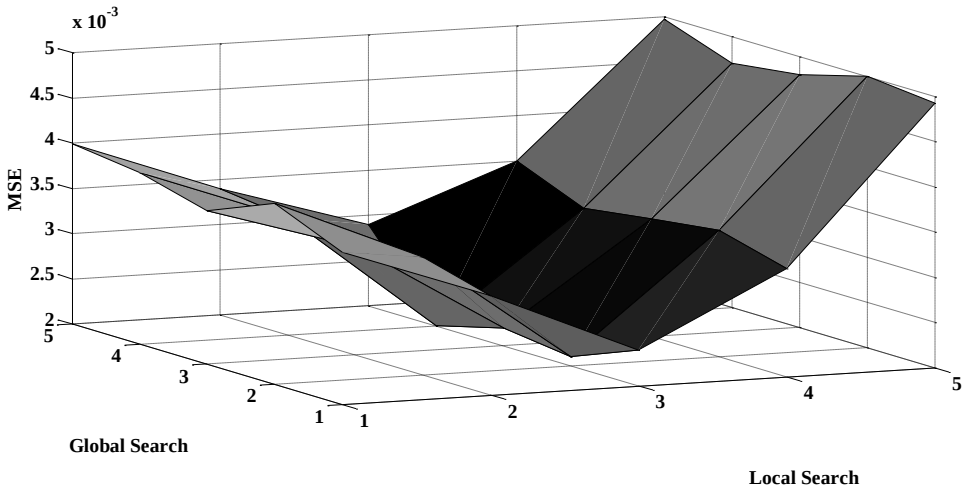


Figure 8. The effect of MSE summing with changing number of the iteration in local and global search space.

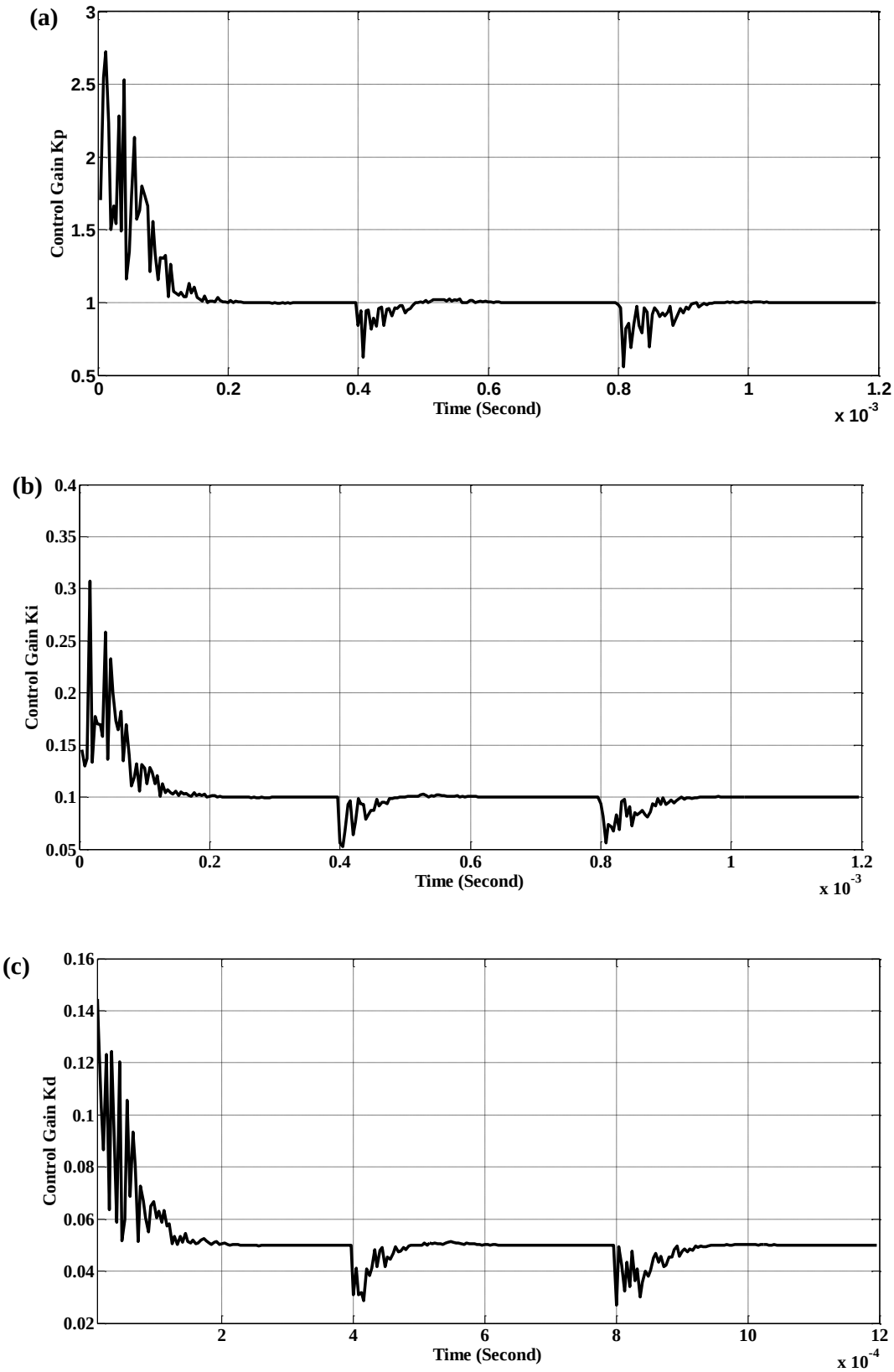


Figure 9. Simulation results of the control parameters (a) kp; (b) kd; (c) ki.

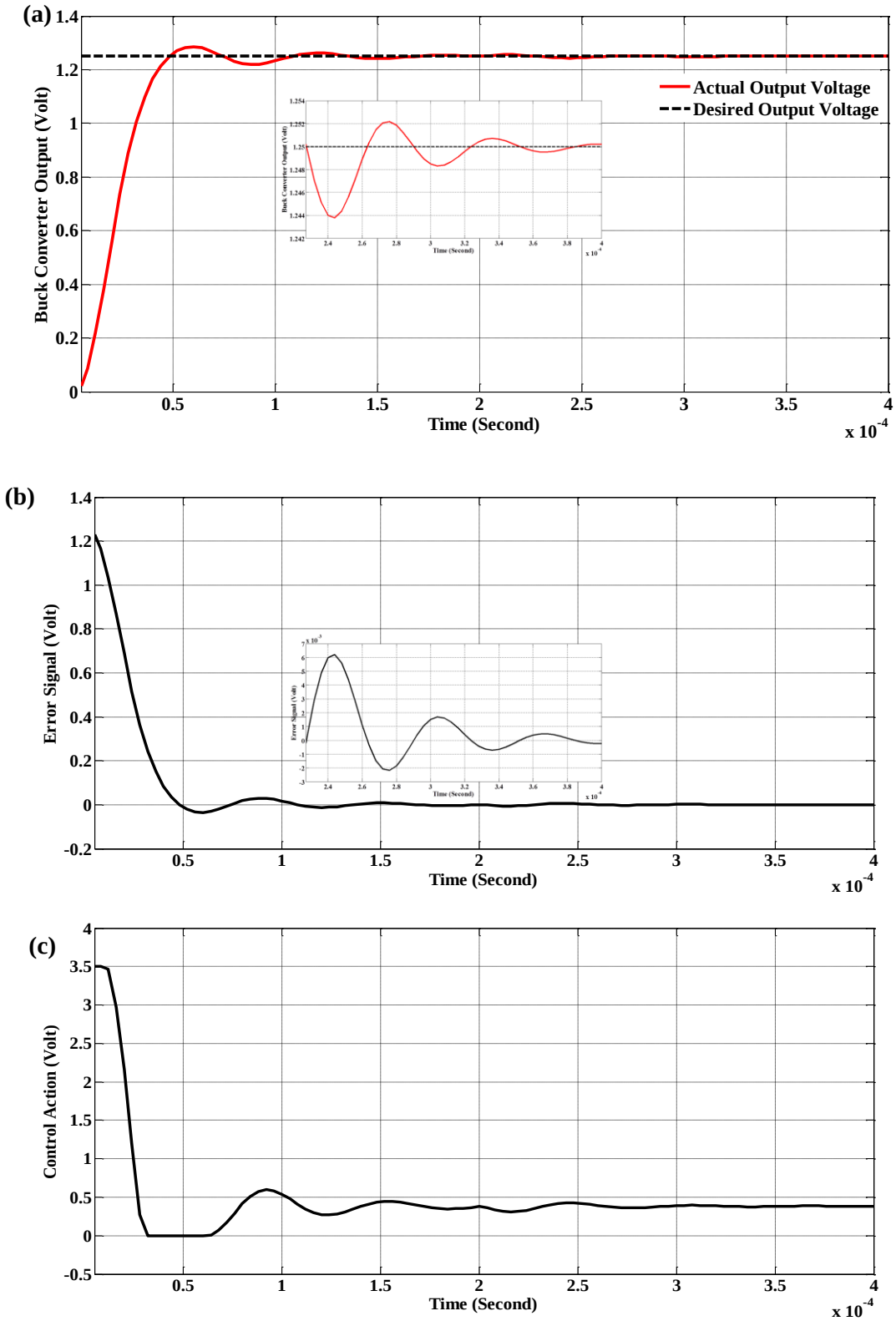


Figure 10. Simulation results of the adaptive PID controller with disturbance effect(a) Output voltage for Buck converter model; (b) Voltage error; (c) Voltage control action.

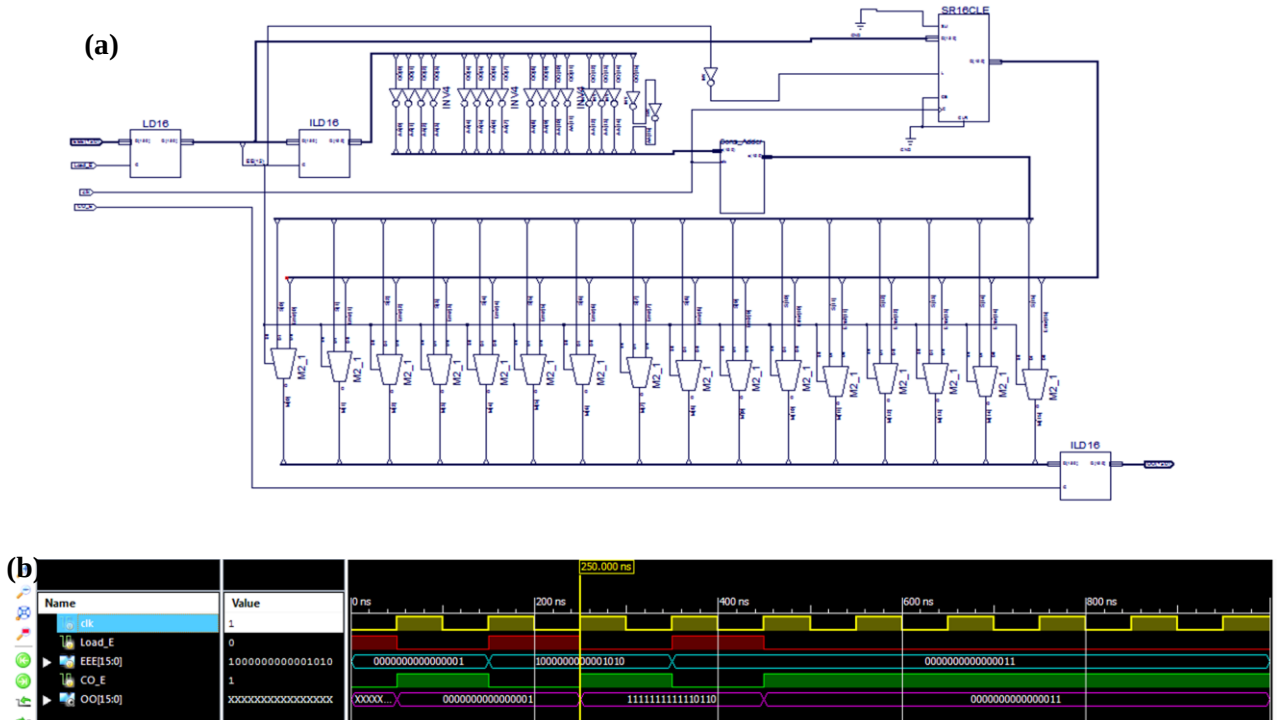
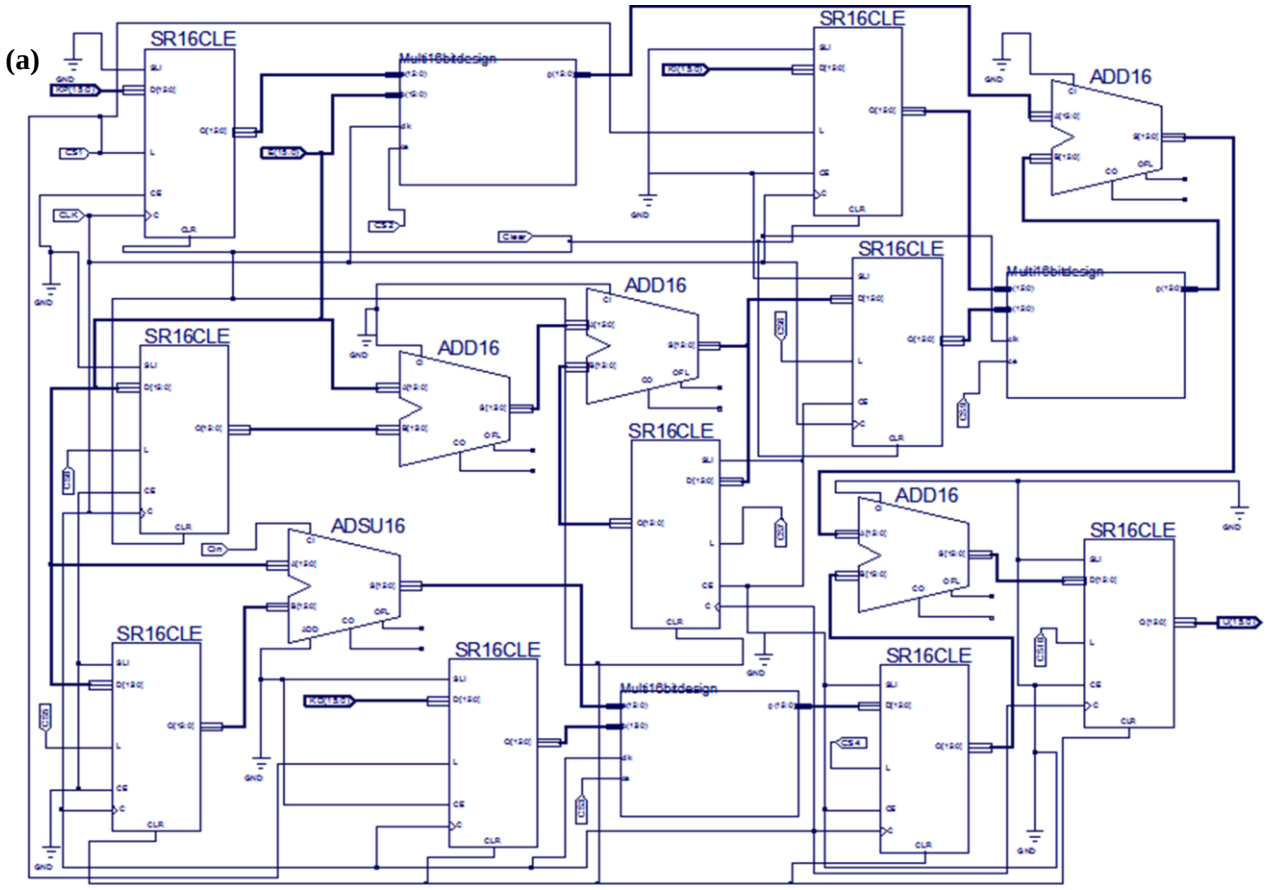


Figure 11. The 2's complement arithmetic digital circuit (a) Schematic diagram; (b) The test bench waveform.



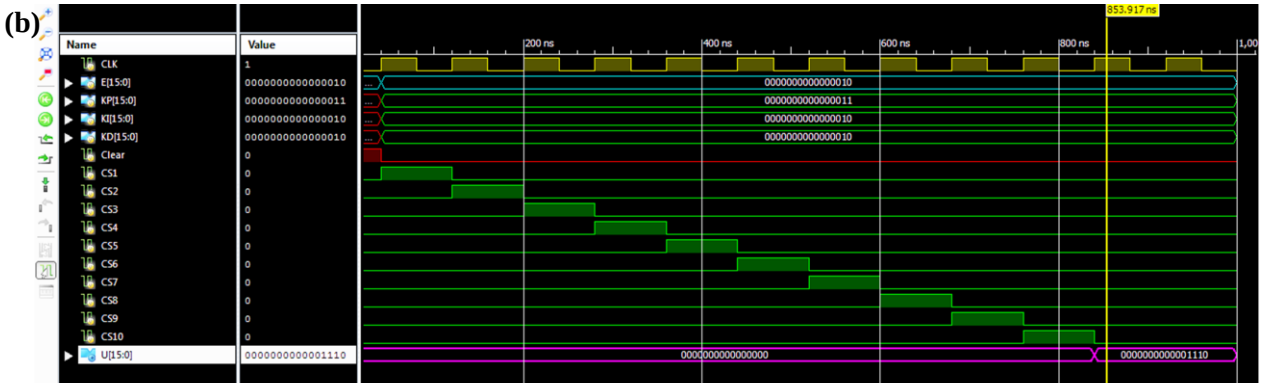
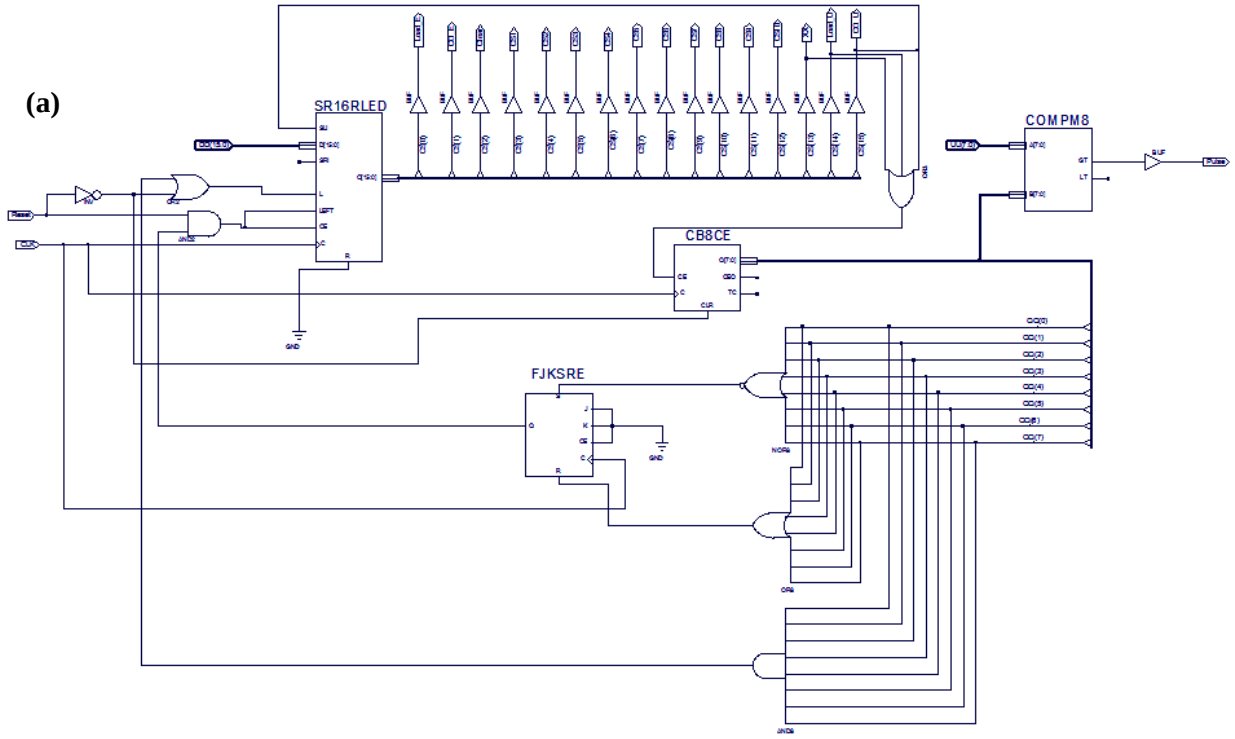


Figure 12. Digital circuit of PID controller (a) Schematic diagram; (b) The test bench waveform.



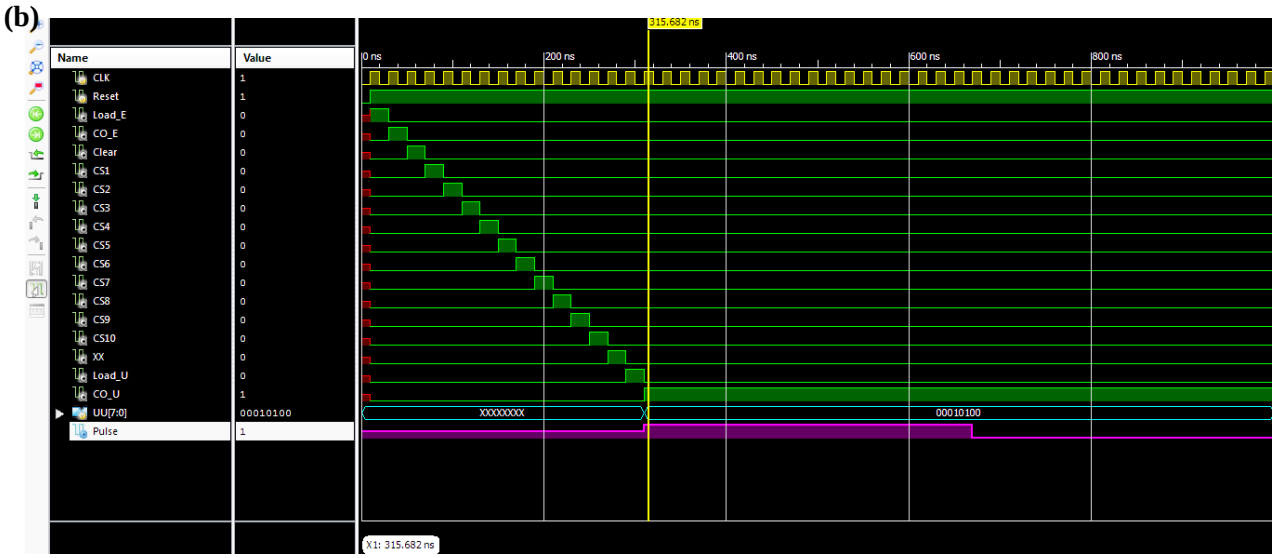
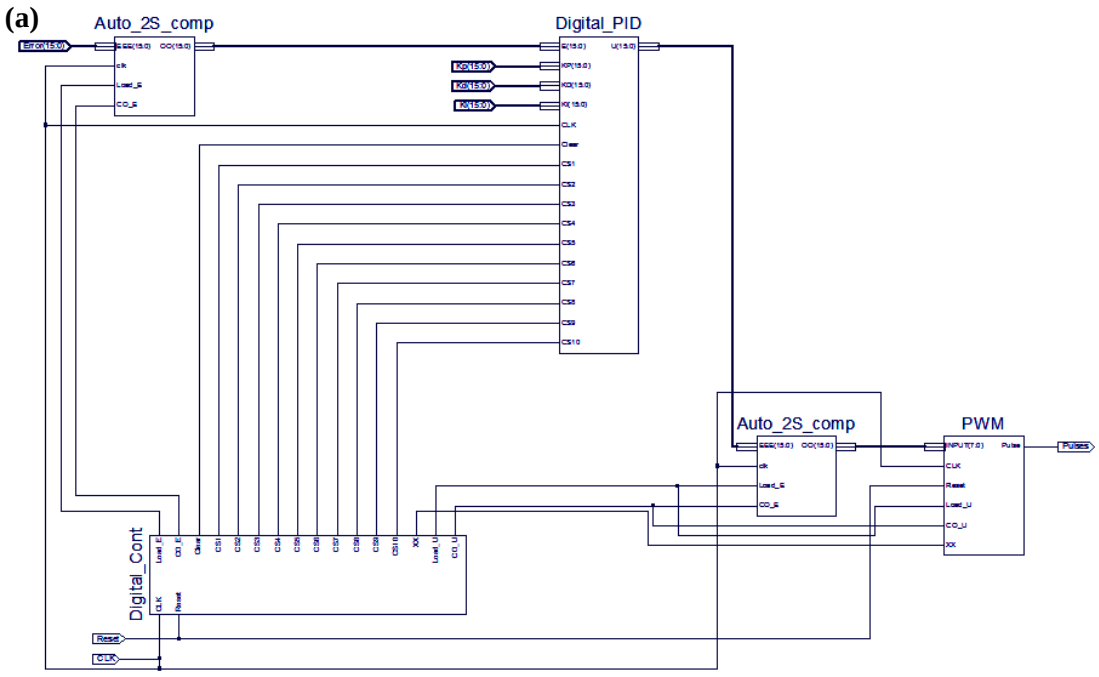


Figure 13. Digital circuit of control unit with PWM digital circuit(a) Schematic diagram; (b) The test bench waveform.



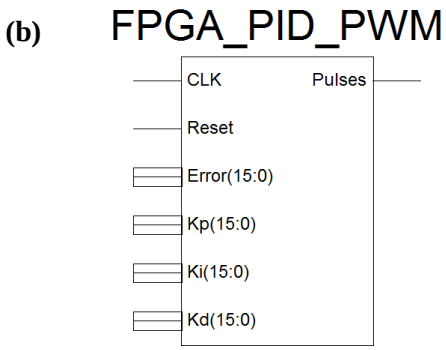


Figure 14. a) The FPGA-PID-PWM controller; b) The top level design of FPGA-PID-PWM IC.

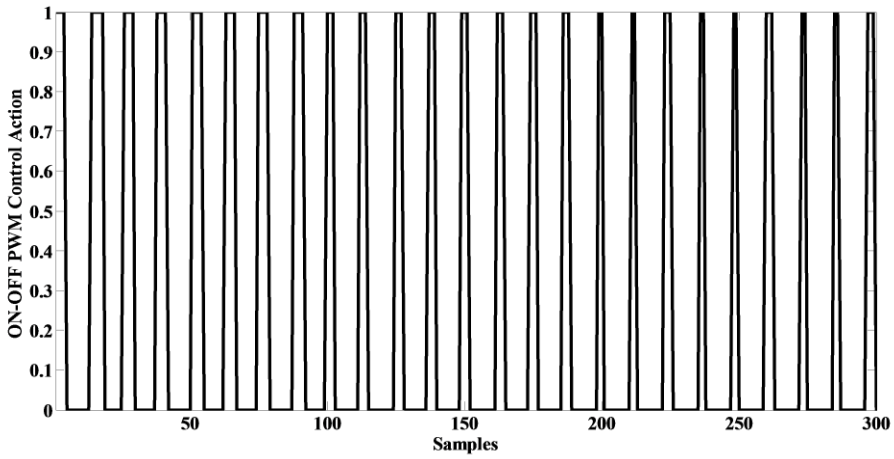


Figure 15. The output of the PWM digital circuit.

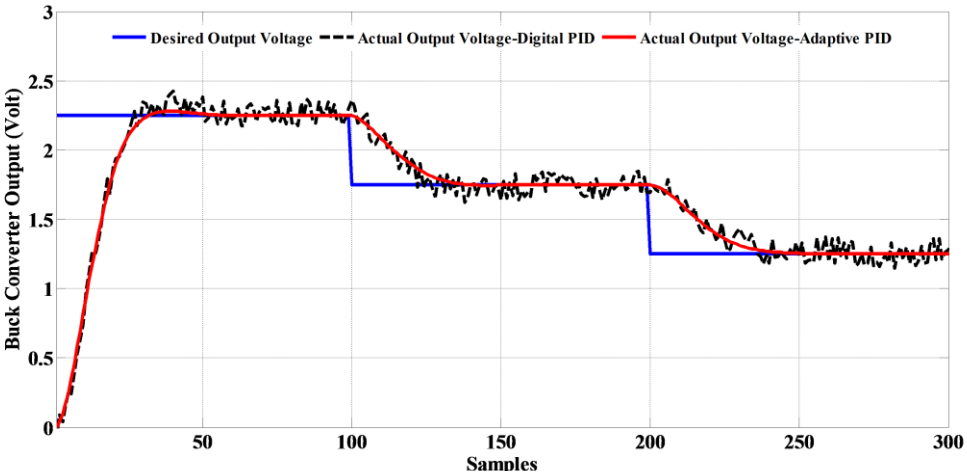


Figure 16. Matlab simulation results and Xilinx ISE results of the output voltage of Buck converter model.

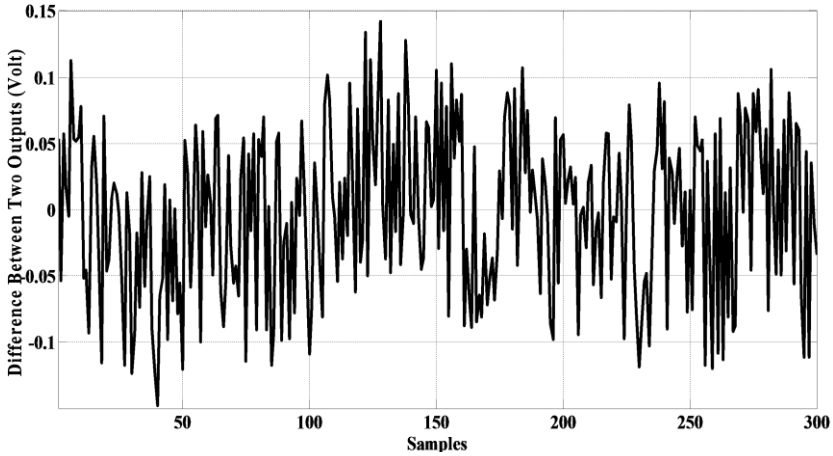


Figure 17. The maximum difference voltage between Matlab simulation result and Xilinx ISE result of the Buck converter output voltage.

Figure 18. Experimental setup of the Xilinx Virtex-5 development system.