

Designing a Secure Software-Defined Radio Transceiver using the Logistic Map

Reem Hashim Ahmed

Researcher

Control and System Engineering Department

University of Technology

Baghdad- Iraq.

reem19952000@gmail.com

Ekhlas Kadum Hamza

Assist Professor

Control and System Engineering Department

University of Technology

Baghdad- Iraq.

ekhlas.k.hamza@uotechnology.edu.iq

ABSTRACT

The need to exchange large amounts of real-time data is constantly increasing in wireless communication. While traditional radio transceivers are not cost-effective and their components should be integrated, software-defined radio (SDR) ones have opened up a new class of wireless technologies with high security. This study aims to design an SDR transceiver was built using one type of modulation, which is 16 QAM, and adding a security subsystem using one type of chaos map, which is a logistic map, because it is a very simple nonlinear dynamical equations that generate a random key and EXCLUSIVE OR with the originally transmitted data to protect data through the transmission. At the receiver, the data will be recovered using the same key, the received data is the same at the sender, so this result shows that the transceiver work normally and calculates the BER at the end each time the SNR changed. Our results indicate that the designed transmitter and receiver perform as usual and finally calculate the bit error rate when the signal to noise ratio is changed. The evaluation of BER indicates that simulated values are smaller than theoretical ones obtained using the BER tool. when SNR is equivalent to 7 dB, the theoretical and simulated BER obtained is 0.01695 and 0.00199, respectively. Designing soft defined radio transceiver using MATLAB R 2011a and system generator ISE14.1/SIMULINK.

Keywords: Software-defined radio, field-programmable gate array, system generator, quadrature amplitude modulation, bit error rate, chaos theory.

تصميم جهاز إرسال واستقبال لاسلكي آمن ومُحدد بالبرمجيات باستخدام مسار منطقي

ا.م.د. اخلاص كاظم
استاذ مساعد

الجامعة التكنولوجية - قسم هندسة السيطرة والنظم

ريم هاشم احمد
باحث

الجامعة التكنولوجية - قسم هندسة السيطرة والنظم

الخلاصة

مع التزايد الكبير في الحاجة الى مختلف انواع الاتصالات من الاتصالات النصية والصوتية والفيديوية والانوية وغيرها فقد اصبحت مسألة تصميم أنظمة جديدة hardware لكل تطبيق جديد مسألة مكلفة ولا تتصف بالمرونة

*Corresponding author

Peer review under the responsibility of University of Baghdad.

<https://doi.org/10.31026/j.eng.2021.06.05>

2520-3339 © 2019 University of Baghdad. Production and hosting by Journal of Engineering.

This is an open access article under the CC BY4 license <http://creativecommons.org/licenses/by/4.0/>.

Article received: 14/8/2020

Article accepted: 22/12/2020

Article published: 1/6/2021



الكافية لمواكبة التطور السريع في العالم. من هنا ظهرت الاجهزة الراديوية (اجهزة الارسال والاستقبال) المعرفة برمجياً والتي يمكن التكهن بمفهومها من اسمها فهي اجهزة hardware يمكن ضبط وتعديل اعداداتها برمجياً للحصول على أنظمة اتصالات مختلفة المواصفات والمديات والتطبيقات فقط بتغيير برمجة هذه الاجهزة. تعتبر الراديويات المعرفة برمجياً او للاختصار (SDR) الاداة الابرز في عالم التصميم والبحث والتطوير العلمي. تهدف هذه الدراسة إلى تصميم جهاز إرسال واستقبال لاسلكي محدد بالبرمجيات من خلال استخدام نوع من التشكيل يُعرف باسم تضمين 16-quadrature amplitude modulation الوقت نفسه، يتم تضمين نظام فرعي مؤمن ويعتمد على chaos map بالإضافة إلى a logistic map. تنتج هذه الخريطة مفاتيح عشوائية وفريدة من نوعها مع المعلومات الأصلية المرسله، وبالتالي حماية المعلومات المرسله. في الطرف المستلم، يتم استرداد المعلومات أيضاً من خلال استخدام المفاتيح العشوائية والحصرية بحيث تكون المعلومات التي تم استلامها مطابقة لتلك التي أرسلها المرسل. تشير نتائجنا إلى أن جهاز الإرسال والاستقبال المصممين يعملان كالمعتاد ويحسبان في النهاية معدل خطأ البتات عند تغيير نسبة الإشارة إلى الضوضاء. يشير تقييم BER إلى أن القيم المحاكاة أصغر من القيم النظرية التي تم الحصول عليها باستخدام أداة BER الكلمات الرئيسية: برمجيات تعريف الراديو، مولد أنظمة، تعديل السعة المربع

1. INTRODUCTION

The SDR transceivers can carry out various tasks based on requirements (**G. Sandhya and Arathyier, 2014**), consequently turning into a stage as models in digital transmission. Thus, this is expressed as a means via which transmission between various tools and applications are set up (**Singh, Sarvpreet, et al., 2017**). The flexible technology of the software-defined radio has led to signals operating digitally (**Simon Haykin, 2005**), allowing for field-programmable gate array (FPGA) to carry out operating signals digitally in real time. However, state-of-art design of gadgets is needed to target field-programmable gate array communication system algorithms (**S. Nassir Hussein, and R. Saad Majeed, 2016**). The reasoning behind substituting conventional radio transceivers with digital ones is the high cost of the equipment and the difficulty in integrating their various components (**Shahad Nafea, Ekhlas Kadum Hamza, 2020**). In other words, SDR transceivers aim to accumulate all the programmable units of material features to build an open design in accordance to the radio system program (**Del Re, Enrico, et al., 2016**).

Most studies were related to SDR transceiver implementation (**Saleim, H. Farhan, 2014**). In this paper, a new network architecture based on the SDN approach is proposed for CRN technology. The authors have shown the advances in unmanned aerial vehicles (UAVs) enable the development of many fields. (**Hien-Lun Peng and Teng-Pin Lin, 2010**) presented an augmented reality (AR) system using the Sequential Wave Imprinting Machine (SWIM) with SDR to visualize electromagnetic phase-coherently (EM) radio waves and other periodic wave phenomena in real-time (**Mann, et al., 2020**).

The software-defined radio is commonly defined as a transmitter and receiver. The fundamental features of radio can be restructured by building on the software and outlining its main characteristics (**Daroon Shaho Omer, et al., 2020**). There are several existing works on the implementation of communication systems using SDR. For instance, the FPGA can be utilized to design a transceiver so that the modulation plan can be effectively changed in accordance with the sensitivity in the channel of communication (**J. Wang, 2019**). This layout can be carried out by utilizing Spartan 3E with a speed of -four as suggested by (**Sajedi, Hedieh, and Mansour Jamzad, 2010**). According to Farhan (**Arjoune, et al., 2018**), efficient programmable transceivers are designed based on SDR technology, offering significant information about implementing the transceivers programmed in Virtex-4 FPGA MB development panel with DAC in P240 Analog Module. So far, many programs and drawing devices



have been utilized to validate the output in terms of conduct, performance, synthesis, scheduling, and zone restrictions(**Saman Atapattu, 2013**).

In this study, a complete SDR transceiver with a security subsystem was designed using chaos theory and the equation of logistic map based on a system generator. This enables to generate a random key of 0 and 1 and mix it with the original data, thus providing the system with enhanced security against any threat (**N. Giweli, et al., 2016**).

The paper is structured as follows: section II describes the architecture of FPGA; section III explains quadrature amplitude modulation (QAM) technique; section IV explains Simulink and system generator, and section V is about the chaos theory. Moreover, sections VI–IX show the results of implementing the SDR on the 16-QAM transceiver, logistic maps, transmitter model, the simulation results, and hardware co-simulation.

2. THE FPGA DESIGN

The field-programmable gate array is made up of a grid of logic blocks and input/output terminal blocks that can be configured. This is shown in **Fig. 1**. Accordingly, by utilizing switches that are programmable and interrelated, digital signals can be generated in the array (**Kumar et al., 2016**). Although the field-programmable gate array processor can carry out fast computations, its memory is restricted (**Chikhaoui Fatima and Djebbari Ali, 2013**). The merits and demerits of the field-programmable gate array when weighing against the application-specific integrated circuit are as below:

- Field-programmable gate array offers a low cost advantage as well as speedier market duration compared with ASICs.
- Although field-programmable gate arrays are flexible, they can be the main factor for their decline. In fact, flexible FPGAs result in higher and lower power consumption than that in ASICs.
- With the aforementioned flaws, FPGAs provide an alternative to the implementation of the digital system because of spending less time in the market and reducing the size of cost.

On the other hand, FPGAs are typically made up of:

- Programmable logic units that perform logic operations.
- Programmable routing, which binds the logical operations.
- I/O sections are joined to the logic blocks through a routing connection, thus making contact outside the chip (**Kolias et al., 2017**).

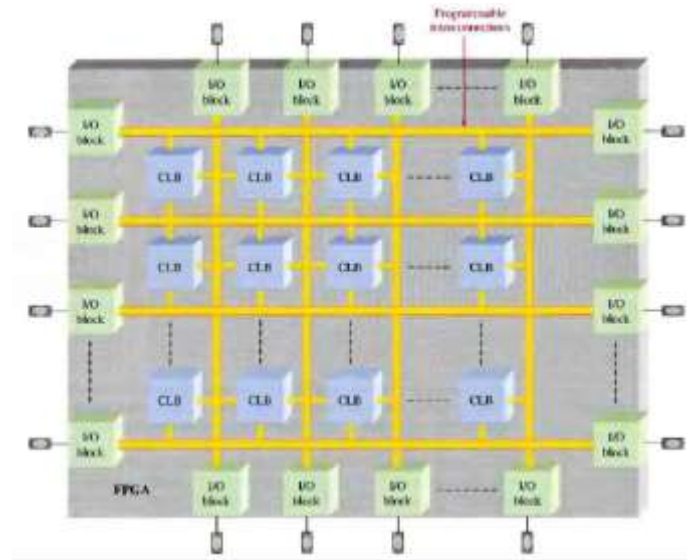


Figure 1. The FPGA basic structure consists of programmable logic units and programmable routing where I/O sections are joined to the logic blocks through a routing connection.

3. QUADRATURE AMPLITUDE MODULATION

Modern systems of the modulation type consider the digital baseband information sent by changing the carrier capacity and frequency. Since capacitance and phase give two degrees of liberty, modulation methods and baseband information are considered by four or more carrier signals, making up Group M (Xiaolong Li, 2008). In the signal scheme of Group M, two or more signals are combined and gathered to make the symbols as well as one of M possible. Thus, during every symbol period, these signals are sent out. The sum of probable signals is given by the equation $M = 2n$, where n is a whole number (Valenzuela, 2015). The M-array modulation method is called ASK, M-array, PSK, or M-array FSK, relying on whether the amplitude, phase, or frequency changes. The Q-M-array modulation changes the amplitude and phase is similar to numerous digital modulation systems (Marwa Mamoun, 2012). QAM is an insertion diagram using two geostationary signals, one of which is 90 degrees off-phase to the other end, transporting data through a physical transmission medium. Since the perpendicular carrier signal operates on a similar frequency range and is different at a 90-degree angle, each signal can be modified and sent separately to the same frequency bandwidth (Md. Saiful Isla et al., 2015). Eventually, it is separated by removing the configuration in the future. For the specified band, quadrature amplitude modulation sends information at double the rate of PAM with no reduction in BER (Jiang, Dingde, et al., 2016).

Henceforth, it is proposed that technology with high-data modulation, for example, the 16-Quadrature Amplitude Modulation, is needed to decode correction of error, for instance, encryption or encryption with turbo so that overlap in the neighboring carrier phase of the 16-Quadrature Amplitude Modulation Plead may be eliminated if it is not minimized (Ivan Abdul-Zahra Hashim, 2015) The quadrature amplitude modulation and its derivatives are both utilized in cellular phones and satellite transmissions. These carrier signals constitute the components of the first phase and the quadratic phase (Q) of our signals.



4. SYSTEM GENERATOR AND SIMULINK

The Xilinx system generator is a MATLAB-Simulink-based planning device for the Xilinx field-programmable gate arrays. Due to this reason, the system generator was then chosen for this particular circumstance, thereby proposing systemizing and providing Simulink mixing components and system generators for simulations. Additionally, the system generator offers self-code generation, which may be loaded on FPGAs from Xilinx (**Sarab Kamal Mahmood, 2014**).

The HDL used throughout for the creation of the code may be determined from the token of the system generator and VHDL or Verilog. The simulations from the system generator are quicker than the conventional HDL simulations, making it simpler for the outcome to be assessed. The system generator utilizes the Xilinx DSP blockset for Simulink and calls the Xilinx Core Generator to spontaneously create extremely enhanced network records for DSP building blocks (**Adrat, Marc, and Gerd Ascheid, 2015**). In this respect, more than ninety DSP building blocks are allowed in the Xilinx blockset for Simulink. These blocks involve popular DSP building blocks, for example, multiples as well as records. Further, a combination of DSP building blocks that are complex in nature is included, for example, front correction of error blocks, Fast Fourier transform, filters and memories (**Umer Farooq et al., 2012**). These blocks benefit from the Xilinx core IP generators to provide improved outcomes for the chosen tool (**Sérgio Bimbi Junior, et al., 2015**).

It should be noted that the system generator block is mandatory for each layout, and the "Gateway In" and "Gateway Out" blocks specify design boundaries translated into an FPGA circle. Format and output values are other common parameters in numerous system building blocks (**Sheela S., and Sathyanarayana S. V., 2017**). Also, custom blocks are also found to exploit the type of information and change its form internally.

5. CHAOS THEORY

Chaos is a periodic behavior that is continuous in an inevitable system, revealing a reliance sensitive to primary situations and standards in fluid flow dynamics created by Lorenz. The chaos theory is about analyzing the conduct of a system that is forceful and sensitive to revisions in its primary conditions. This occurrence is usually known as the butterfly effect. Thus, minor revisions in its initial conditions may result in extensively different outcomes, making future forecast difficult for these powerful systems (**A. I. Mecwan, and N. P., Gajjar, 2011**). Theoretically, the anarchist system can create an unlimited quantity of chaotic signals, which are recurring and having the character of high-speed internet access. These characteristics make these signals especially important transmissions that are secure. The principles of chaos may be utilized in numerous areas as given below (**Reddy, Bathula Siva Kumar, 2018**):

- Field of Engineering like a turbine, vibration control, energy, chemical reaction, lasers, and grids.
- Computers, packages switches in computer systems, and data security (encryption).
- Data processing encrypt data and decrypt data while also storing it in chaotic systems. It is likewise utilized in neural networks to enhance efficiency and recognize patterns.
- Synchronization for safe communication as well as broadband radio mayhem. It is also utilized to encrypt data modification.

Chaotic systems are grouped into two categories: i) chaotic map and ii) chaotic flow (M. Cicioğlu, S. Cicioğlu, and A., Çalhan, 2018).

i) Chaotic map

The chaotic map has an evolutionary role, which offers a kind of conduct that is chaotic. Anarchic maps can be selected at a separate duration so that separate maps generally take the form of repetitive k th operations, occurring in the research of dynamic systems as follows:

$$x_k = f(x_{k-1}) \quad (1)$$

whereby x_k is the case vector and $f(\cdot)$ presents the constant function known as a chaotic map, notably, logistic map and quadratic map. The logistic map gives an idea of the occurrence of extremely complicated conduct from very basic nonlinear dynamical equations, followed by the random behavior of the system (Chikhaoui Fatima and Djebbari Ali, 2013). Arithmetically, the logistic map is expressed below:

$$x_n = r * x_{n-1} * (1 - x_{n-1}) \quad (2)$$

whereby x_n is between 0 and 1, and $0 < r < 4$ is called the bifurcation parameter.

Overall, the binary sequence is produced by utilizing the logistic map. This is illustrated in the flowchart of Fig. 2.

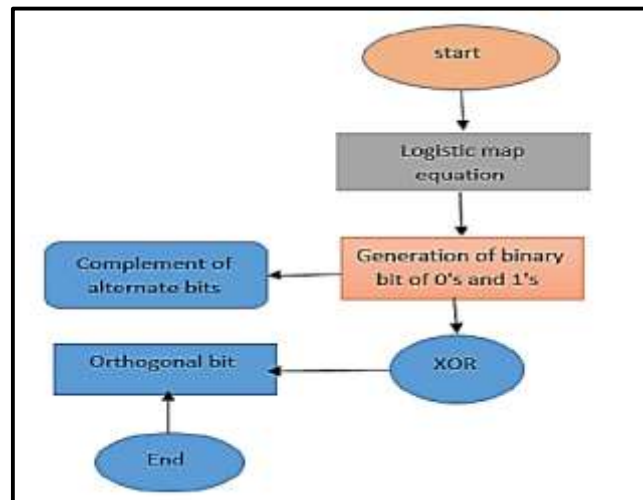


Figure 2. The flowchart of the orthogonal logistic map.

6. IMPLEMENTATION OF SOFTWARE-DEFINED RADIO FOR 16-QAM TRANSCEIVER

The transmitter and receiver system of 16-Quadrature Amplitude Modulation was executed according to the IEEE 802.11.a specification using a frequency band of 24 GHz. The signals entering the system were assumed to be in binary form by default. Figure 3 displays the general entity of the system's execution, involving the transmitter.

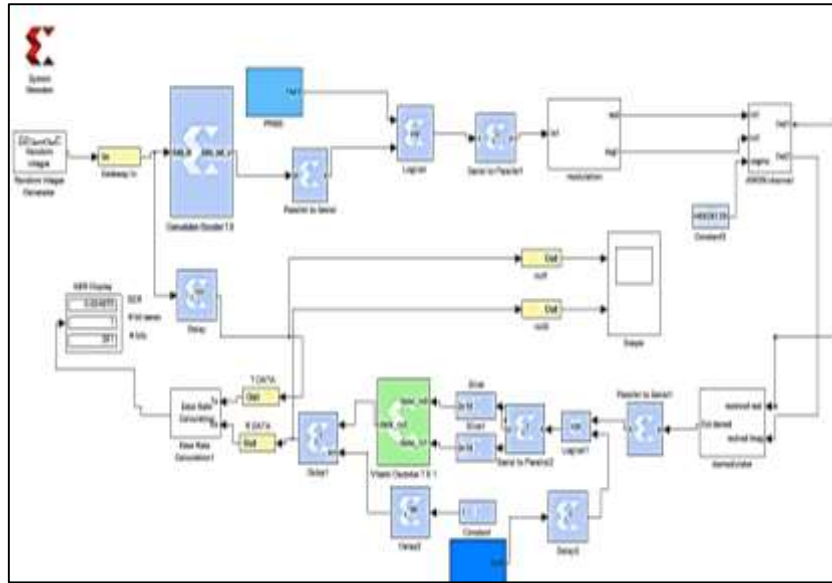


Figure 3. Xilinx Software-Defined Radio transceiver.

The Bernoulli binary generator randomly generated the input bit stream in Simulink. It was then altered to Xilinx fixed point through Gateway In. Figure 4 presents details of the output wave of the binary generator.

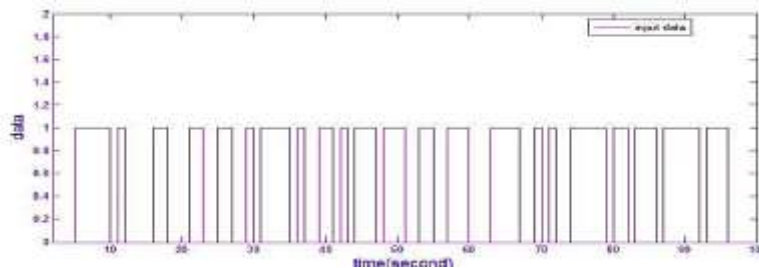


Figure 4. The input data stream from a binary generator.

6. TRANSMITTER MODEL

After the input data sequence is produced, the information is entered in the convolutional encoder performing with rate half, constraint length of three, and code array 171 and 133, (poly2trellis (7, [171 133])). For example, a stream data [1000 1 1] and the information after encoding procedure through the convolutional encoder are [11110100 110], as displayed in the diagram below. With this execution, the issues or mistakes in the Additive White Gaussian Noise channel are solved while including redundancy.

Message=[1000 1 1]

Output=[11110100110]

After the encoding process, the data is entered in the parallel to serial method and the resulting serial information is found to be [0 0 0 0 0 1 1 1 1 0 1 0 0 1 1 0 0 0 1 0 1], according to Fig. 5. PRBG is obtained according to Eq. (1) in the previous section. This equation is



changed to Xilinx system generator with the following primary conditions: $xn = 0.99$ and $r = 4$, as shown in **Fig. 6**.

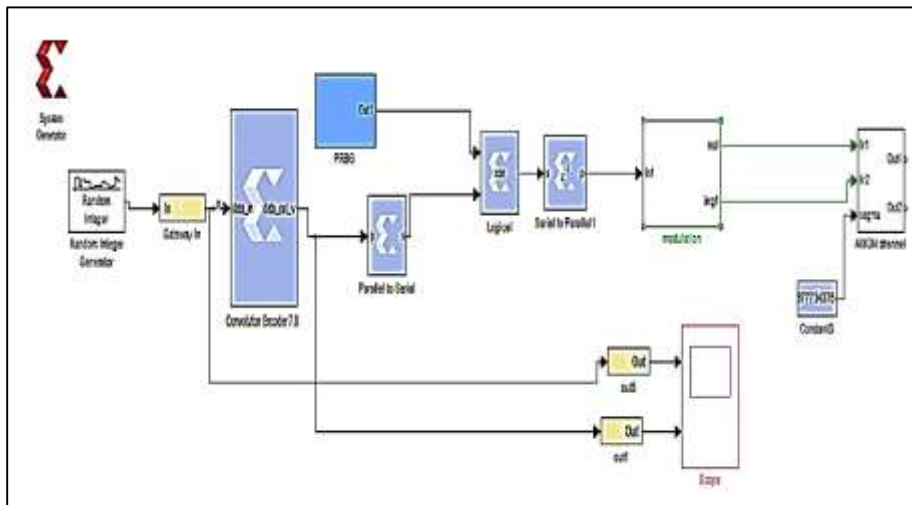


Figure 5. Xilinx 16-QAM Software-Defined Radio transmitter.

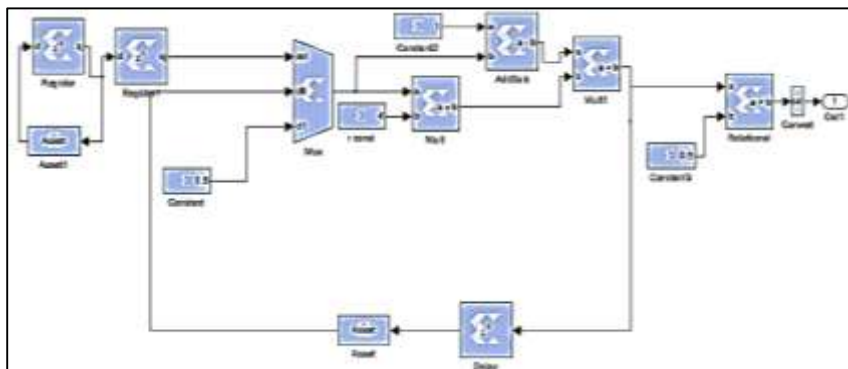


Figure 6. Xilinx PRBG subsystem.

The information created by the logistic map [1 1 1 1 1 0 0 0 0 0 1 1 0 0 0 1 1 0 0 ...] in **Fig. 4** is entered in the logical process, thereby making the data sent most safe by the redundant bit of the key produced by PRBG. Therefore, the data after this procedure is found to be [1 1 1 1 0 0 1 1 0 1 0 0 0 0 0 0 1 0 1 0 0 1 ...] as depicted in **Fig. 7(a)**.

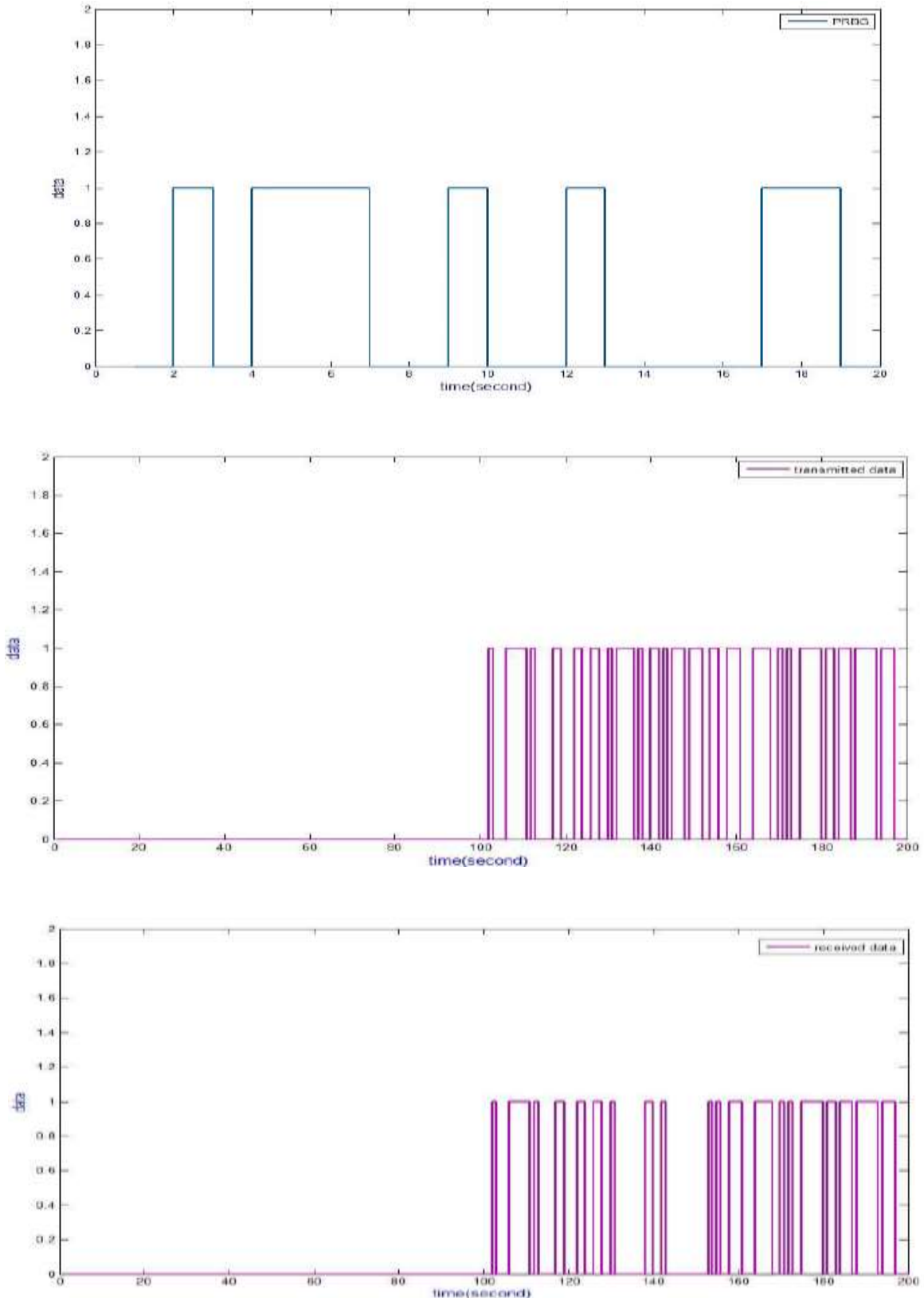


Figure 7. (a) Output data of PRBG, (b) transmitted data, and (c) receiving data.



Fig. 7(b) and **7(c)** show the input signal to the dispatcher and the produced signal. When the two signals coincide with each other, the input and output signals after the wait of about 100s are identical to the system characteristics discussed above, and the receiving signal is decrypted without any major error.

7. SIMULATION RESULTS

The suggested SDR transceiver system performance was resolved when passing during the proposed medium, and the simulated BER was compared with the theoretical one. The results obtained are presented in **Fig. 8**. As inferred from the BER curve with the AWGN channel, any increase in values improves the corresponding Bit Error Rate efficiency. Also, it is found that the system simulated with the 16-QAM Software-Defined Radio performs more satisfactorily than the theoretical system. For example, when SDR is equivalent to 7 dB, the theoretical and simulated BER obtained is 0.01695 and 0.00199, respectively.

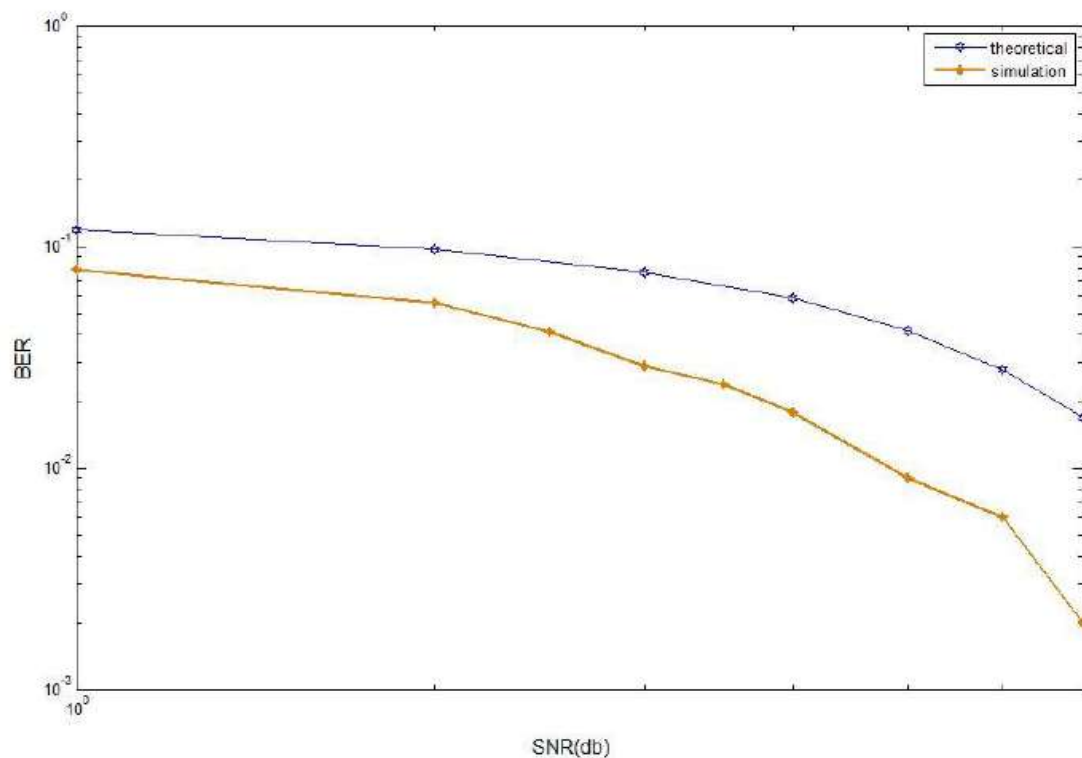


Figure 8. Theoretical and simulated Bit Error Rate as a function of SDR.

8. Co-Simulation Of Hardwar

The configuration of the system generator was carried out by using a field-programmable gate array in a Simulink simulation scenario, thus, establishing the usefulness of the system and creating results in the hardware utilized for the composed amount. This approach is called the co-simulation of both hardware and software. In many studies, it has been taken into consideration, performing the usefulness of the system based on field-programmable gate array.

With regards to the Xilinx program kits, installing the Ethernet connectivity (JTAG) by utilizing the 3A starter board (as implemented in **Fig. 2**) compresses the hardware of the recent Xilinx



library for one block. This first block involves most of the occupation for the system applied to the FPGA kit and is associated with the bitstream loaded in the FPGA. At the point the co-simulation begins, the bitstream is stacked initially and, through JTAG connectivity, sends the inputs of Simulation to the kits. Then, the output is read in return for JTAG, which is directed to Simulink. Thus, the results shown are used to compare the simulated result with the expected output and produce a VHDL code for the system generator. However, this system competes with the downstream to generate a field-programmable gate array file. In the following subsection, hardware policies of the 16-QAM modulator are described and compared with the earlier results.

i) Co-simulation of Software-Defined Radio transmitter

This layout is altered by performing a common simulation through some procedures to obtain the final design of the desired quadrature amplitude modulation transmitter model 16, according to **Fig. 9(a)**.

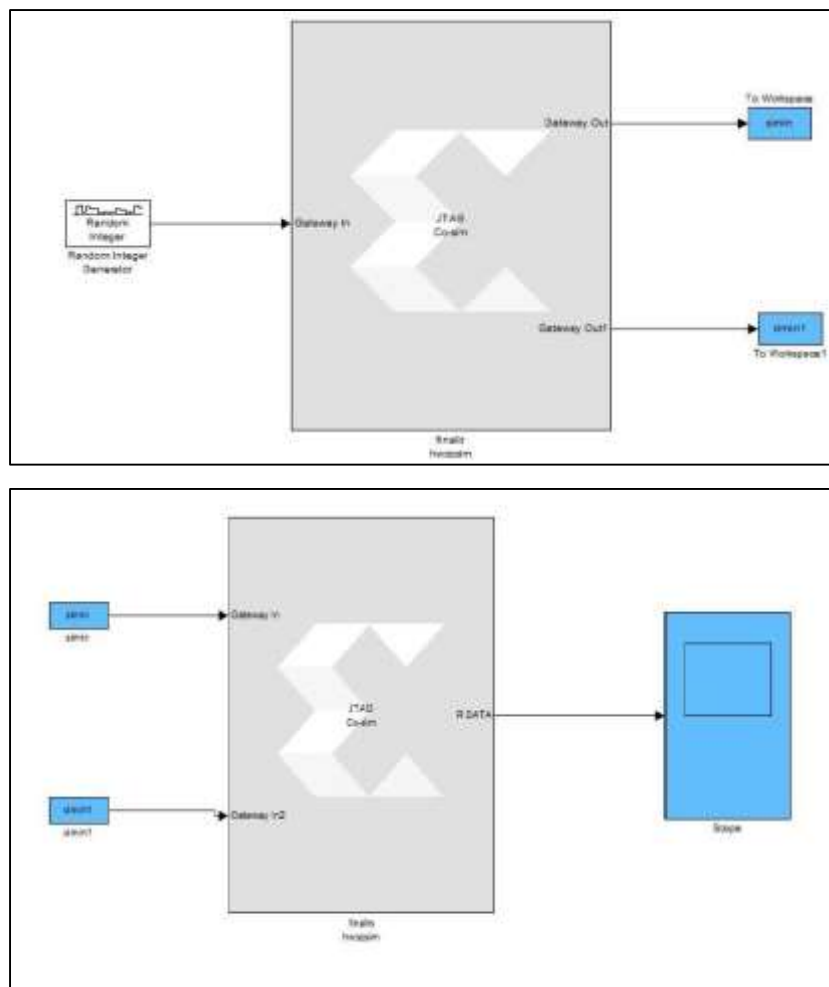


Figure 9. (a) SDR transmitter hardware co-simulation and (b) SDR receiver hardware co-simulation.



ii) Software-Defined Radio receiver model

The layout of this receiver model is carried out in a similar way as the transmitter. In this regard, **Fig. 9(b)** presents the complete compilation.

9. CONCLUSIONS

In summary, a procedure for executing the Software-Defined Radio transceiver according to IEEE 802.11. a was designed. This was separated into phases. Every phase included certain steps to simulate the parts of the Software-Defined Radio transceiver and the system generator. Various notes were taken into consideration when locating the system's efficiency by checking the allowed error rate measurement results. The transmitter and receiver systems of the 16-QAM Software-Defined Radio were structured by utilizing MATLAB / Simulink 2011a, thus, demonstrating the likely implementation under IEEE 802.11.a. The latest security for chaos was made by utilizing the system generator, which gave a random key to enhancing information security for foreseeable applications. The simulation results showed that the recommended 16-QAM transmitter has much better results when sending to an Additive white Gaussian noise channel with the energy of bit to noise values ranging from 0 dB to 10 dB. The BER of the system was found to range between 10^{-1} and 10^{-3} when displaying the AWGN channel. Nevertheless, the transmitter and receiver gave more than satisfactory results. The BER values were permanently zero for the field energy of bit to noise that is 8^{-10} dB at around 1000 bits. This means that the simulated Bit Error Rate showed lower numbers than those of theoretical BER obtained by the BER tool. The transceiver was done by utilizing the Field-programmable gate array-Spartan 3A and formed Register Transfer Level simulation for each part of the transceiver.

REFERENCES

- G. Sandhya and Arathyiyer, 2014. A prototyping Of Software Defined Radio Using QPSK Modulation', International Journal Of Electronics And Communication Engineering & TECHNOLOGY (IJECE), Volume 5, Issue 12, pp. 130-138.
- Singh, Sarvpreet, Marc Adrat, and Gerald Ulbricht, 2017. Special Issue on Increasing Flexibility in Wireless Software Defined Radio Systems, Journal of Signal Processing Systems 89.1: 81-83.
- S. Nassir Hussein and R. Saad Majeed, 2016. Design and FPGA implementation of wireless baseband modem for wimax system based on SDR, J. Eng. Dev., vol. 19, no. 06, pp. 184–197.
- Shahad Nafea, Ekhlas Kadum Hamza, 2020. Design and Analysis WIMAX Network Based on Coverage Planning. Journal of Engineering Number 2 Volume 26 February.
- Del Re, Enrico, et al., 2016. Future wireless systems for human bond communications, *Wireless Personal Communications* 88.1: 39-52.
- Saleim Hachem Farhan, 2014. Design and Implementation of Programmable Transceivers Based Software Defined Radio Using FPGA, International Journal of Recent Technology and Engineering (IJRTE).



- Hien-Lun Peng and Prof. Teng-Pin Lin, 2010. Integrating FPGA with Multi-Core SDR Development Platform to Design WiMAX Baseband System, Department of Industrial Design, Tatung University.
- S. Mann, P. V., Do, Z. Lu, and J. K. K. Lau, 2020. Sequential Wave Imprinting Machine (SWIM) Implementation using SDR, Seventh International Conference on Software Defined Systems (SDS).
- Daroon Shaho Omer, et al., 2020. Ergodic Capacity for Evaluation of Mobile System Performance" Journal of Engineering Number 10, Volume 26, October.
- Sajedi, Hedieh, and Mansour Jamzad, 2010. Using contourlet transform and cover selection for secure steganography, *International Journal of Information Security* 9.5: 337-352.
- Chikhaoui Fatima, and Djebbari Ali, 2013. New chaotic binary sequences with good correlation property using logistic maps, *IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*, Volume 5, Issue 3, PP 59-64.
- Koliass, Constantinos, Vasilis Koliass, and Georgios Kambourakis, 2017. TermID: A distributed swarm intelligence-based approach for wireless intrusion detection, *International Journal of Information Security* 16.4: 401-416.
- Xiaolong Li, 2008. Simulink-based Simulation of Quadrature Amplitude Modulation (QAM) System, *IAJC-IJME International Conference* ISBN 978-1-60643-379-9.
- Valenzuela, Michael, Ferenc Szidarovszky, and Jerzy Rozenblit, 2015. A multiresolution approach for optimal defense against random attacks, *International Journal of Information Security* 14.1: 61-72.
- Marwa Mamoun Abdel Gadir Abdel Rahman, 2012. Software Defined Radio, thesis submitted to the University of Khartoum.
- Md. Saiful Islam, Md. Hasan Rahman, and Jakeya Sultana, 2015. Performance Analysis of QAM+ and QPSK in AWGN and Multipath Fading Channel, *International Journal of Advanced Research in Computer Science and Software Engineering*, Bangladesh University.
- Jiang, Dingde, et al., 2016. Collaborative multi-hop routing in cognitive wireless networks, *Wireless personal communications* 86.2: 901-923.
- Ivan Abdul-Zahra Hashim, 2015. Automatic Digital Modulation Identification for Software Defined Radio Based on FPGA, thesis, Department of Electrical Engineering, University of Technology.
- Sarab Kamal Mahmood, 2014. Chaos Based Channel Coding" a thesis submitted to the Electrical Engineering Department, College of Engineering, Al-Mustansiriya University.
- Adrat, Marc, and Gerd Ascheid, 2015. Special issue on recent innovations in wireless software-defined radio systems." *Journal of Signal Processing Systems* 78.3: 239-241.
- Umer Farooq, Zied Marrakchi, and Habib Mehrez, 2012. Tree-based Heterogeneous FPGA Architectures: Application Specific Exploration and Optimization, Springer-Verlag New York.
- Sérgio Bimbi Junior, Vitor Chaves de Oliveira, and Gunnar Bedicks Junior, 2015. Software Defined Radio Implementation of a QPSK Modulator/Demodulator in an Extensive Hardware Platform Based on FPGAs Xilinx ZYNQ, *Journal of Computer Science*, Brazil.



- Sheela S and S. V. Sathyanarayana, 2017. Application of chaos theory in data security- a survey, Department of Electronics and Communication Engineering, JNNCE, Shimoga, Karnataka.
- I. Mecwan and N. P. Gajjar, 2011. Implementation of Software Defined Radio on FPGA, International Conference, IEEE.
- Reddy, Bathula Siva Kumar, 2013. Experimental Validation of Timing, Frequency and Phase Correction of Received Signals Using Software Defined Radio Testbed, Wireless Personal Communications 101.4: 2085-2103.
- M. Cicioğlu, S. Cicioğlu, A. Çalhan, 2018. Performance analysis of software-defined network approach for wireless cognitive radio networks, 26th Signal Processing and Communications Applications Conference (SIU).
- J. Wang, Y. Liu, S. Niu, H. Song, 2019. Integration of Software Defined Radios and Software Defined Networking Towards Reinforcement Learning Enabled Unmanned Aerial Vehicle Networks, IEEE International Conference on Industrial Internet (ICII).