

The Design and Simulation of a Novel Optical Adder Depending on Optical Tri-state Gates

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ABSTRACT

Essential approaches involving photons are among the most common uses of parallel optical computation due to their recent invention, ease of production, and low cost. As a result, most researchers have concentrated their efforts on it. The Basic Arithmetic Unit BAU is built using a three-step approach that uses optical gates with three states to configure the circuitry for addition, subtraction, and multiplication. This is a new optical computing method based on the usage of a radix of (2): a binary number with a signed-digit (BSD) system that includes the numbers -1, 0, and 1. Light with horizontal polarization (LHP) (\leftrightarrow), light with no intensity (LNI) (\odot), and light with vertical polarization (LVP) (\updownarrow) is represented by -1, 0, and 1, respectively. This research proposes new processor designs for addition. As a result, the design can achieve m addition operations with an operand length of n bits simultaneously. To explain and justify the theoretical design idea, the three steps of adding a BSD are numerically simulated. The constructing process is thought to be more precise and faster because the time to add does not depend on the length of the word. For all entries, all bits are implemented simultaneously, boosting the system's efficiency. A simulation model for six addition processes with a total bit count of 15 bits across all entries is presented in this work performing in a one-time parallelism manner.

Keywords: The Basic Arithmetic Unit(BAU), Optic Gates with Three States, Binary Signed Digit Number (BSD) system, Addition process, Algorithm of Three-step Addition.

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تصميم ومحاكاة الجامع الضوئي الجديد اعتمادا على البوابات الضوئية الثلاثية الحالة

علاء الصفار أستاذ مساعد كلية التقنية الهندسية / الجامعة التقنية الهندسية الجنوبية	عيسى احمد عبد أستاذ مساعد كلية التقنية الهندسية/ الجامعة التقنية الهندسية الجنوبية	* قبيلة قاسم ثابت دكتورة وزارة التربية/مديرية تربية البصرة
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الخلاصة

تعد الاساليب التي تتضمن التونوات احد اكثر التطبيقات شيوعا للحساب البصري المتوازي نظرا لظهورها الحديث وسهولة الانتاج والكلفة المنخفضة. نتيجة لذلك، ركز غالبية الباحثين اهتمامهم عليه. تم انشاء وحدة الحساب الاساسية BAU باستخدام خوارزمية ثلاثية الخطوة تستخدم بوابات ثلاثية ضوئية لتكوين الوائر الحسابية لعملية الجمع والضرب وهذه طريقة حوسبة ضوئية جديدة يعتمد على اعتماد الرقم الثنائي المؤشر -1، 0، 1، حيث ان -1 يمثل الضوء المستقطب أفقيا أما ال0 يمثل العتمة او الظلام بينما 1 يمثل الضوء المستقطب عموديا. ويقترح اهذا البحث تصميمات معالج جديدة لاداء عمليات الجمع. وبالتالي التصميم ينجز m من العمليات الحسابية الخاصة بالجمع بطول كلمة مقدارها n بت. تمت المحاكاة لتنفيذ ستة عمليات جمع في ان واحد يتم ادخال البيانات ومعالجتها لذا تتم العمليات بغض النظر عن طول المعاملات مما يعزز كفاءة النظام، وقدمنا هنا نموذج للجمع جميع المعاملات يتألف من 10 بت.

الكلمات الرئيسية: الوحدة الحسابية الاساسية، البوابات المنطقية الضوئية ثلاثية الحالة، النظام الرقمي الثنائي المؤشر، عملية الجمع، الخوارزمية ثلاثية الحالة.

1. INTRODUCTION

Despite digital computers' claims of great advances in performance, reliability, and scalability, they are unable to keep up with the rapid development of computer design and power consumption, highlighting the need for optical computers (Cherri, et al., 1998, and Alaa A. Al-Saffar, et al., 2014). Due to that, the insulators in the electronic equipment are lower ticklish to cross-talk and not get short circuits, which is why the optical equipment does not want that material. In the optical equipment, different frequencies of light can be transferred at the same time with no intrusion (Augustus E. Ibhaze, et al., 2020). This will help the device photonic to manage the train of data simultaneously in a simple manner. Nowadays, the computing speed can be improved by larger than 7 orders of magnitude using optical computing. Utilizing classical computers requires 12 years of processing equal to one hour with optical computer architecture (H. Abdeldayem, et al., 2008, T. Chattopadhyay, et al., 2008, J. Yi et al., 2010). Many researchers looked at construct using several types of digital computation systems, such as residue-number system (Ch. Jiang, et al., 2010), multiple values fixed in form radix-number system (V. Patel, et al., 2010), redundant numbers (Q. Abu Al-Haiha, et al., 2010), and a type of number system called signed digit representations, that allows parallelism arithmetic operations has fewer carry propagation steps (H. A. Kamal, et al., 2004, R. Rani, et al., 2009, and W. Yassin, et al., 2010). Jin Yi (J. Yi, et al., 2003, Yan Junyong, et al., 2008, J. Yi, et al., 2010 and O. Shan, et al., 2010) suggested a design method for ternary optical computer construction that uses polarization and intensities to indicate ternary (three) values: {0,1,2}. In this research, the field of digital computing has also expanded to include the employment of neural networks (Anwar Dhyaa Majeed, et al., 2021, and Qabeela Q. Thabit, et al., 2021).



A new design is introduced by using three-state optical gates as a raw material to build the computational circuit based on the three-state algorithm, thus introducing a new paradigm for parallel addition operations. In previous research, it was not used or used only as an adjuvant.

The building block in the presented design is an additional unit (the smallest synthetic unit called Basic Arithmetic Unit BAU), a signed number system using a three-step approach based on three-state optical gates.

Many other sections in this paper can be listed as follows: The background information in Section II covers the binary number system, the three-step technique, and the concept of three-state optical gates. The third section explains the construction of the gates and how they work, and the proposed algorithm. The simulated visual results are presented in the fourth section. Conclusions and recommendations for future work are found in Section 5.

2. THE RELATED WORK

Due to the benefits that optical calculations provide, such as parallel processing of incoming signals, which will be represented in the form of light polarization, as well as the lack of interference between optical devices and the advanced method of work using signed-digit number systems that are higher than traditional digital systems, where digital indicator systems were introduced (SHen Yunfu, et al., 2021). The application of the three-step algorithm in the implementation of additional operations, which works with signed numbers, provides the benefit of carrying the residual to the next rank with the option of parallel addition so that all operations for all bits are done at the same time (Junjie Peng, et al., 2019). A triple optical computer (TOC) combines two polarized lamps with orthogonal polarization states and an empty light state, then rotates the polarization direction of the light using a device such as a liquid crystal pixel array to display the information. It can include millions of processor bits for some processes. TOC has several advantages, including easy processor scalability, huge processor bits, bit assignment ability, bit reconfiguration, parallel computing, and low power consumption, which makes it more suitable for processing vast amounts of data with complex processes (Song Kai, 2011 and Goutam Mandal, 2019). Recently, the artificial bee colony algorithm has been linked to the parallel design of the triple optical computer (Shuang Li, et al., 2019).

3. BACKGROUND

3.1 Binary Signed-digit Number (BSD)

A class of number impersonation system can be supplied using the binary modified signed-digit number (BMSD). Binary signed-digit number (BSD) can be boundary load obstetrics to one place on the left within the process of subtraction and addition in the digital computer. Utilizing the operand redundant structure, the load generation chains are neglected (R.S. Fyath, et al., 2004). The integer- radix ($radx > 1$) is with the impersonation of a classical number, where every digit is allowed to assume punctually r values $(0, 1, \dots, r - 1)$. The goal of using (BMSD) impersonation is to declare summation operation and subtraction operation of two operand number without serial obstetrics required through the adder, where the time period of the operation is free of the operands length. It can be similar to the subtraction or addition time of dual digits. In BSD number, the decimal number is (M.S. Alam, et al., 1994): -

$$Dec = \sum_{j=0}^{n-1} X_j \text{ radx}^j \quad (1)$$

Dec = Decimal number.

X_j = In BSD, it is the j th digit

Where $X_j \in \{-\alpha, \dots, -1, 0, 1, \dots, \alpha\}$, $\alpha \leq r - 1$.



radx= Is radix of number in BSD.

n = Represents the digit number in BSD.

3.2 Algorithm Procedure of Three-step

Based on the number of steps, Modified Signed Digit (MSD) addition algorithms are divided into three types: one-step, two-step (M.S. Alam, et al., 1994), and three-step (Alaa A. Al-Saffar, et al., 2018). The advantages and disadvantages of one-step and two-step algorithms are outlined below: fewer stages, but optical execution becomes more complicated. As a result, for ease of optical implementation, a three-step approach was adopted in this study. Let's have a look at the form of MSD structure of augend X with addend Y:

$$(X)_{MSD} = (x_{n-1}, \dots, x_i, \dots, x_0).$$

$$(Y)_{MSD} = (y_{n-1}, \dots, y_i, \dots, y_0).$$

The algorithm of (3) moves acting addition operation is achieved depending on the sequence following steps:-

Step(1): Calculate

$$(X_i + Y_i = 2T_{i+1} + W_i \quad (i=0, \dots, n-1)) \tag{2}$$

where :-

(T) :- represent carry value of two operands.

(W) :- represent sum value of two operands.

Every pair of two bits of first number X_i and the second one Y_i of the two numbers MSD numbers addition have T- transformation and W- transformation are given in following Table 1 and Table 2, as the following (Qabeela Q. Thabit, et al., 2019):

Table 1. Step one (T- carry transformation) truth table(Qabeela Q. Thabit, et al., 2019).

T	1	0	-1
1	1	1	0
0	1	0	-1
-1	0	-1	-1

Table 2. Step one (W- sum transformation) truth table(Qabeela Q. Thabit, et al., 2019).

W	1	0	-1
1	0	-1	0
0	-1	0	1
-1	0	1	0

Step (2): In this step, we calculate

$$(T_i + W_i = 2T'_{i+1} + W'_i \quad (i=0, \dots, n-1)) \tag{3}$$

Approximately, every pair of two bits of operand results T_i and W_i obtain T'_{i+1} and W'_i (T'-transformation and sum W'-transformation) as explained in Table 3 and Table 4.



Table 3. Step two(T'-carry transformation) truth table(Qabeela Q. Thabit, et al., 2019).

T'	1	0	-1
1	1	0	0
0	0	0	0
-1	0	0	-1

Table 4. Step two (W'-sum transformation) truth table(Qabeela Q. Thabit, et al., 2019).

W'	1	0	-1
1	0	1	0
0	1	0	-1
-1	0	-1	0

Step (3): Finally, we calculate

$$(Sum_i = W'_i + T'_i \quad (i=0, \dots, n-1)) \tag{4}$$

As indicated in the T-transformation rule presented in Table 1, the final value of the sum S_i truth table on everyone pair of two bits have of operands T'_i and W'_i (S. Y. Fu, et al., 2011). Because addition is a fundamental operation in all arithmetic operations, speeding up addition speeds up the entire arithmetic process. As a result, researchers have worked to create a suitable parallel carry-free addition and a computer representation of numbers mechanism that can speed up addition (T. Imam, et al., 2005). The three-step MSD addition method is depicted in Fig.1. As indicated in the diagram, T&W, T'&W', and T are the three types of functional blocks (FBs) used in addition; each is accomplished in steps 1, 2, and 3. Because there are so many optical processor units to use in the execution process, each of the aforementioned stages can be implemented in parallel on the optical adder experimental platform.

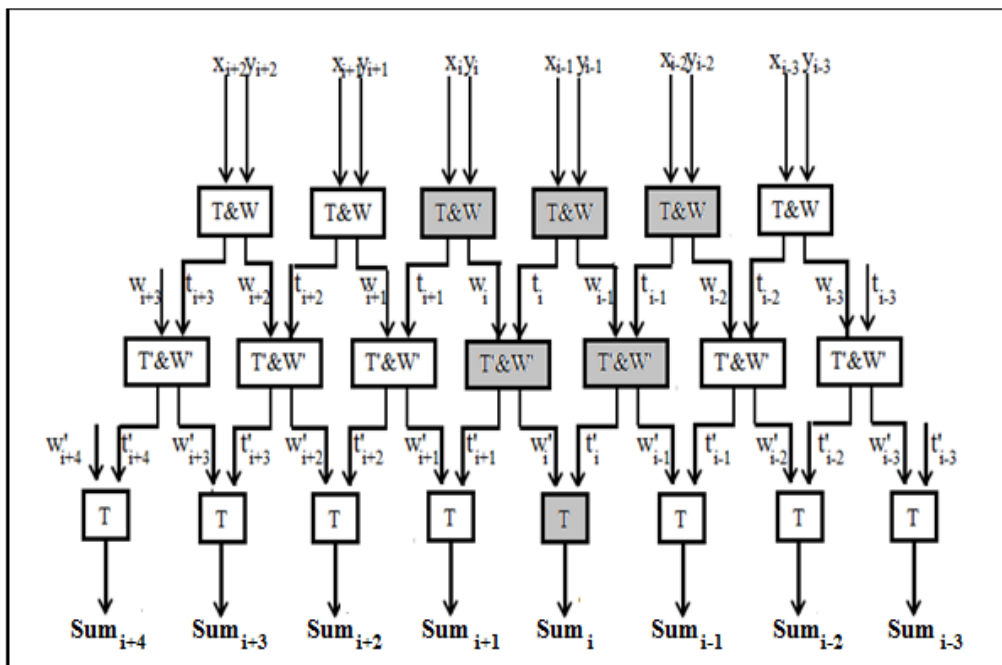


Figure1.The structure of three-type of functional blocks (Alaa A. Al-Saffar, et al., 2017).

3.3 Concept of mechanism of Tri-state Optical Gates Working

In the digital system, the logic gates are considered as the constructing bulk. The light ray can be monitored by another one in the whole optical logic gate, which is doing as a switch and no demand electrical signal. In that case, when the device produces light, it is (ON), and when the device does not create light, it is (OFF).

We can investigate the group of tri-state logical states in optical implementation $\{-1, 0, \text{ and } 1\}$, -1 is light that is horizontally polarized (LHP) (\leftrightarrow), 0 is light of no intensity (LNI) (\odot), and 1 is light that is vertically polarized (LVP) (\updownarrow). Table 5 shows the truth tables for various tristate logic operations. (T. Chattopadhyay, et al., 2008, and A. Raja, et al., 2020).

Table 5. Optical (Three-State) logical process truth tables

- (a) Trinary-gates(OR, AND, and XOR), (b) Inverter (Tri-State) gate, Truth (Tri-State) Detector gate, False (Tri-State) Detector gate (T. Chattopadhyay, et al., 2008, and A. Raja, et al., 2020).

B	A	OR	AND	XOR
-1	-1	-1	-1	1
-1	0	-1	0	-1
-1	1	0	0	0
0	-1	-1	0	-1
0	0	0	0	0
0	1	1	0	1
1	-1	0	0	0
1	0	1	0	1
1	1	1	1	-1

(a)

A	Inverter Gate	True Detecor TD Gate	False Detecor FD Gate
-1	1	0	-1
0	-1	1	0
1	0	1	-1

(b)

4 SUGGESTED ADDITION ALGORITHM STRUCTURE

4.1 Step-One Addition (Carry Transformation(T)):

From **Table 1**, explain step-one addition T-transformation results in value (1) in only three cases of addition ((1+1), (1+0), and (0+1)), while rest cases results in outputs value (-1) in ((-1+-1), (-1+0), and (0+-1)) as seen in **Fig. 2**, are created using an OR optical gate.

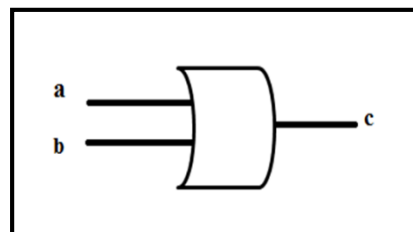


Figure 2. OR use an optical gate.

4.2 Step-One Addition (Sum Transformation(W)):

Backing to **Table 2**, explain step-one addition W-transformation results in value(-1) only if adding combinations ((1+0), and (0+1)) while combinations that produce in outputs value (1) in two addition cases ((-1+0), and (0+-1)) As shown in **Fig. 3**, the following optical gates in combination are used to create these designs.

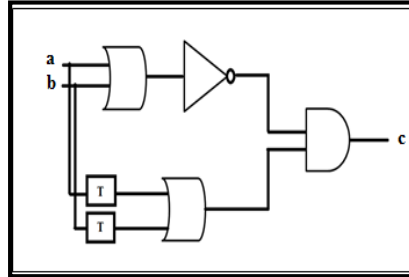


Figure 3. W-Sum Transformation using a combination optical gates circuit.

4.3 Step-Two Addition (Carry Transformation(T')):

Backing to Table 3, the result of the second T'-carry transformation is 1 in just one case (1+1), whereas the result in outputs is -1 in one case (-1+1) as illustrated in **Fig. 4**.

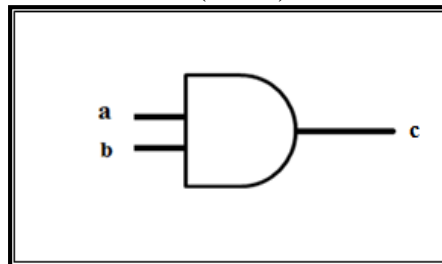


Figure 4. AND there's an optical gate.

4.4 Step-Two Algorithm (W'- Sum Transformation):

Table 4 shows that the step two W'- sum transformation produces outputs of 1 in just two situations (1+0) and (0+1), and outcomes of -1 in two adding cases (-1+0) and (0+-1) when employing the combination optical gates shown in **Fig. 5**.

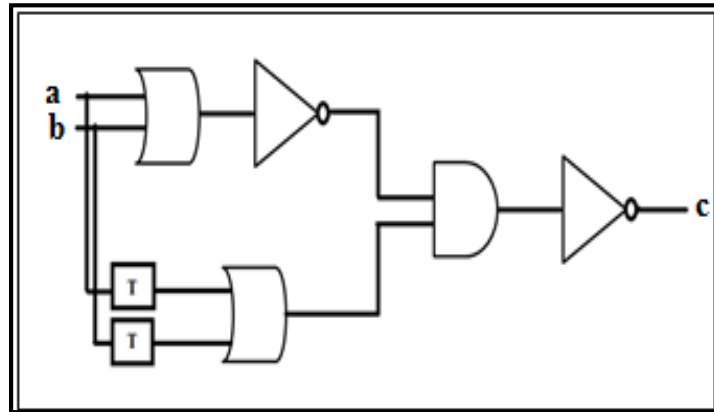


Figure 5. W'-Transformation is performed using a combined optical gates circuit.

4.5 Step-Three Algorithm (T- Carry transformation):

The T- carry transformation is employed in case three to obtain the final sum's findings; the T-transformation from the previous stage is applied in this step. As shown in Fig. 6, the foregoing circuits are combined to form a single basic arithmetic unit (BAU) that performs one-bit addition for X and Y.

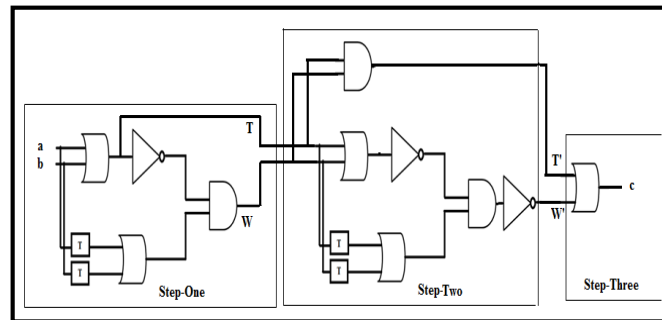


Figure 6. The arithmetic unit is a basic arithmetic unit (BAU).

The adder's structure is made up of m-blocks that represents operations number, each of which comprises n-BAU which that represents word in bits' length, allowing every block must be able to deal with a pair of numbers with n bits each. The addition is done in parallelism performance together with many number pairs at the same time. As a result, all processes are completed at the same time, boosting the system's efficiency. Fig. 7 depicts the processing procedure in all blocks at the same time.

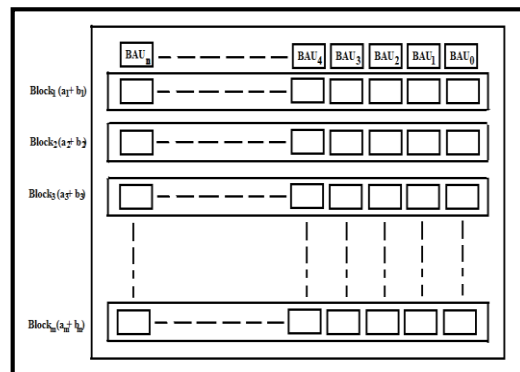


Figure 7. Optical adder's architecture.



5 THREE-STEP ADDER OPTICAL SIMULATION

To complete the simulation process, the Visual Basic VB programming language was used, where each operation was accomplished with a series of basic arithmetic units, the number of units here is n for one operation, while the total number of operations is m, all of these operations enter parallel to the logical processing, in other words, all operations answer can be got simultaneously. For example, consider the following addition operation: - number 6 is used to denote the number of operations as above mention is represented No. of blocks m. Every process has 2 operands, each one including (15 bits each) that reflect the unit numbers called basic arithmetic unit (n) in every one of a block. The simulation of these processes is explained in **Fig. 8**; the results or final sum in step three in each operation can be read from right to left.

Operation(process)1

$$a_1 = (-27803)_{10} = (-1-1-10011100-1-1-101)_{\text{BSD}}$$

$$b_1 = (28188)_{10} = (111000-1-1-1-1-11100)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (000000-100110000-1)_{\text{BSD}}, T_1 = (00000100-1-1-100010)_{\text{BSD}}$$

$$\text{Step two: } W_2 = (000001-10-1000001-1)_{\text{BSD}}, T_2 = (000000000000000000)_{\text{BSD}}$$

$$\text{Step three: } C_1 = (385)_{10} = (000001-10-1000001-1)_{\text{BSD}}, \text{ represent in row(1) in Fig8.}$$

Operation(process)2

$$a_2 = (32767)_{10} = (111111111111111)_{\text{BSD}}$$

$$b_2 = (0)_{10} = (000000000000000000)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (0-1-1-1-1-1-1-1-1-1-1-1-1-1-1)_{\text{BSD}}, T_1 = (111111111111111)_{\text{BSD}}$$

$$\text{Step two: } W_2 = (100000000000000000-1)_{\text{BSD}}, T_2 = (000000000000000000)_{\text{BSD}}$$

$$\text{Step three: } C_2 = (32767)_{10} = (100000000000000000-1)_{\text{BSD}}, \text{ represent in row(2) in Fig8.}$$

Operation(process)3

$$a_3 = (-4136)_{10} = (00-1-111111100-1-1-1)_{\text{BSD}}$$

$$b_3 = (32644)_{10} = (111111111-1-1-1-100)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (0-1-10000000011011)_{\text{BSD}}, T_1 = (1100111110-1-1-1-1-10)_{\text{BSD}}$$

$$\text{Step two: } W_2 = (10-10111110-100-101)_{\text{BSD}}, T_2 = (000000000000000000)_{\text{BSD}}$$

$$\text{Step three: } C_3 = (28509)_{10} = (10-10111110-100-101)_{\text{BSD}}, \text{ represent in row(3) in Fig8.}$$

Operation(process)4

$$a_4 = (-7789)_{10} = (00-1-1-1-100-1-1-10011)_{\text{BSD}}$$

$$b_4 = (3780)_{10} = (000111100-1-1-1-100)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (0001000-1010011-1-1), T_1 = (00-100010-1-1-1-1-1110)$$

$$\text{Step two: } W_2 = (00-11001-1-10-1-1000-1), T_2 = (00000000000000001000)$$

$$\text{Step three: } C_4 = (-4009)_{10} = (00-11001-1-10-1-1100-1)_{\text{BSD}}, \text{ represent in row(4) in Fig8.}$$

Operation(process)5

$$a_5 = (30224)_{10} = (111100-1-1-1-1-10000)_{\text{BSD}}$$

$$b_5 = (30291)_{10} = (111100-1-1-110-1-10-1)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (000000000000011101)_{\text{BSD}}, T_1 = (111100-1-1-10-1-1-10-10)_{\text{BSD}}$$

$$\text{Step two: } W_2 = (111100-1-1-10-1001-11)_{\text{BSD}}, T_2 = (00000000000000001000)_{\text{BSD}}$$

$$\text{Step three: } C_5 = (60515)_{10} = (111100-1-1-10-1001-11)_{\text{BSD}}, \text{ represent in row(5) in Fig8.}$$

Operation(process)6

$$a_6 = (27656)_{10} = (11100-1-1-1-1-1-1-1000)_{\text{BSD}}$$

$$b_6 = (-24846)_{10} = (-1-1-111110000-1-1-10)_{\text{BSD}}$$

$$\text{Step one: } W_1 = (0000-1-10011110110)_{\text{BSD}}, T_1 = (0001100-1-1-1-1-1-1-100)_{\text{BSD}}$$

$$\text{Step two: } W_2 = (00010-10-10000-1010)_{\text{BSD}}, T_2 = (00000000000000001000)_{\text{BSD}}$$



Step three: $C_6 = (2810)_{10} = (00010-10-10000-1010)_{BSD}$, represent in row(6) in Fig8.

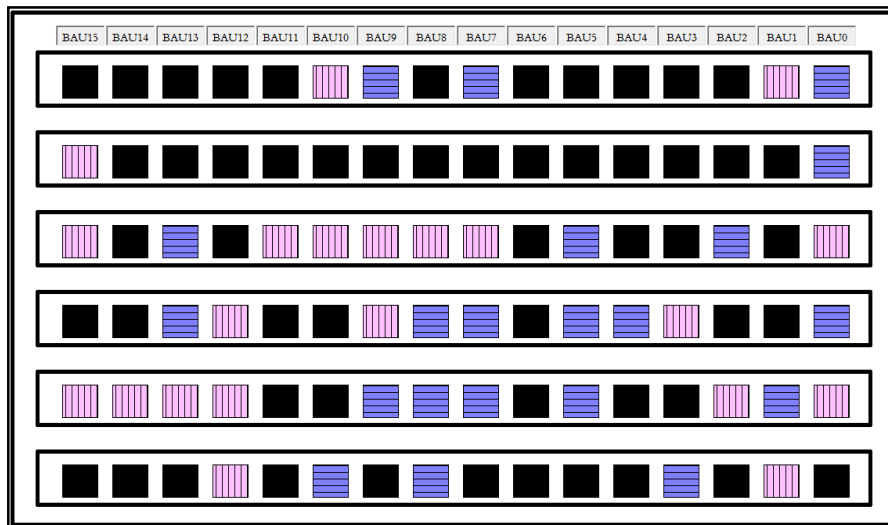


Figure 8. Simulation results in each operation.

6 CONCLUSIONS

Optically computation is a new way of thinking about how computers work today. The principle behind this technology is still improving and gaining traction, even though it isn't generally available or mass-produced yet. Optical computing is an emerging type of computing that uses optical components to do computations using appropriate algorithms. All scientists in any discipline concentrate on the advantages of any proposed design. Performance, affordability, stability, flexibility, parallelism implementation, and precision are all important factors that consider the top priorities. One of the useful conclusions that we have reached is the employment of triple gates to build efficient designs with the possibility of applying all indicative and non-indicated digital systems to perform mathematical operations. This represents an expansion in the field of optical computing. The fundamentals of optical computer architecture are discussed. This may be accomplished by employing updated computer developed by using 3-state optical gates to handle the binary type of number which that signed digit number systems as optic signals. A brief overview of the study's history and tools is provided, and a simulation model based on Visual Basic language programming.

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