GENERATION OF MPSK SIGNAL USING LOGIC CIRCUITS

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ABSTRACT:

The traditional technique of generating MPSK signals is basically to use IQ modulator that involves analog processing like multiplication and addition where inaccuracies may exist and would lead to imbalance problems that affects the output modulated signal and hence the overall performance of the system. In this paper, a simple method is presented for generating the MPSK using logic circuits that basically generated M-carrier signals each carrier of different equally spaced phase shift. Then these carriers are time multiplexed, according to the data symbols, into the output modulated signal.

الخلاصة:

التقنيات التقليدية لتوليد اشارة MPSK هي اساساً تستخدم مضمن IQ الذي يحوي على عمليات تناضرية مثل الضرب والجمع حيث توجد عدم الدقة مما يؤدي الى مشاكل عدم التوازن التي تؤثر على اشارة الاخراج المضمنة وبالتالي على الاداء الكلي للمنظومة. في هذا البحث تم تقديم طريقة مبسطة لتوليداشارة MPSK باستعمال دوائر منطقية حيث اساساً تولد عدد M من الاشارات الحاملة كل واحدة بتزحيف طور مختلف وموزعة بالتساوي. ثم يتم انتقاء احدى هذه الاشارات الحاملة حسب رموز البيانات لتتولد الاشارة المحملة.

INTRODUCTION

Phase-Shift Keying is one of the basic digital modulation schemes in which the digital data are modulated into discrete equally spaced phase shift values of the carrier signal. The number of these discrete phase shift values represents the number of levels of the PSK modulation that is generally referred to as MPSK or M-ary PSK. For the two special cases where M=2 and M=4, the modulation is referred to as Binary PSK (BPSK) and Quadrature PSK (QPSK) respectively. For higher values of M it is referred to as 8PSK, 16PSK, and so on.

In practice BPSK and QPSK are much widely used than 8PSK and 16PSK because the complexity of the system is much higher and since basically, the M-ary PSK and the M-ary QAM have similar spectral bandwidth and system complexity, and the fact that the performance of the QAM modulation is better in terms of probability of error for the same average transmitted signal power, the QAM modulation is preferred and more widely used than MPSK. On the other hand, one advantage in favor of the MPSK over the QAM is that the MPSK has constant envelope while the QAM does not have constant envelope. Therefore the superior performance of the M-ary QAM can be realized only if the channel is free from nonlinearities.

MPSK and QAM modulations are basically implemented using IQ modulator. Imbalance in the I and Q branches is a common problem in the IQ modulator and various techniques were introduced to overcome this problem. In-phase and quadrature amplitudes and phase imbalances are caused by the analog components of the modulator [1].

Cho et al. [1] provided an expression for the probability of symbol error of MPSK-OFDM signal with IQ imbalance over AWGN channel in terms of 2-D Gaussian Q-function, the formula obtained was verified by simulation results. Park et al. [2] worked on the symbol-error probability (SEP) of MPSK signals in the situation of phase error, quadrature error and in-phase-quarature (I-Q) gain mismatch, in the presence of AWGN and fading channel using Moment Generating Function (MGF) approach. No counter measures were provided both [1] and [2]. Schuchert et al. [3] presented a simulation of an adaptive equalizer applied to OFDM based Digital Video Broadcast-Terrestrial (DVB-T) system. The equalization process is applied to each subcarrier of the OFDM and the coefficients are adapted using data aided training sequence. The equalizer corrects both the channel distortion and IQ imbalance. Nemer et al. [4] presented an algorithm for IQ balancing based on a blind estimation of the magnitude and phase imbalances from the correlation functions of the received I and Q channels without the need of training sequence. The algorithm is further simplified by approximation to eliminate the division operations and reduce the number of multiplication operations and to put it in the form of two cascaded iterative feedback schemes, the first for the magnitude correction and the second for the phase correction. Simulation was applied to DVB signal with QPSK, 8PSK and 16-QAM constellations. Liu [5] presented a study on the IQ imbalance at both the transmitter and the receiver of OFDM systems. A time domain self-calibrating of IQ imbalance estimator for the transmitter is suggested that estimated the amplitude and phase using a training sequence. At the receiver, the estimator of the amplitude and phase imbalance is based on correlation equation of the FFT output of the receiver. The receiver estimator does not rely on training sequence. The performance is evaluated using simulation against AWGN and multipath Rayleigh fading channel.

IQ IMBALANCE

Although there are different formulas of expressing the amplitude and phase imbalance in quadrature modulation but actually these formulas are basically the same and the difference is only as a matter of convenience in choosing the proper mathematical expression. One of these formulas for expressing the amplitude and phase imbalance in a general quadrature modulation (MPSK or QAM) is [4]

$$\begin{bmatrix} I' \\ Q' \end{bmatrix} = \begin{bmatrix} 1+\varepsilon & 0 \\ 0 & 1-\varepsilon \end{bmatrix} \begin{bmatrix} \cos(\Delta\phi/2) & -\sin(\Delta\phi/2) \\ -\sin(\Delta\phi/2) & \cos(\Delta\phi/2) \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} \quad (1)$$

Where I' and Q' are imbalanced in-phase and quadrature-phase components of the modulated signal, and I and Q are the balanced in-phase and quadrature-phase components, and ε and $\Delta\phi$ are the amplitude and phase imbalance factors respectively. Equation (1) can be expressed without the matrix form as

$$I' = (1+\varepsilon)\left[\cos(\Delta\phi/2)I - \sin(\Delta\phi/2)Q\right] \quad (2a)$$

$$Q' = (1-\varepsilon)[\cos(\Delta\phi/2)Q - \sin(\Delta\phi/2)I] \quad (2b)$$

It should be noted that ε and $\Delta\phi$ are not time dependent factors although they are in general frequency dependent factors [6].
An expression for a multilevel PSK signal can be represented in any of these forms

$$s(t) = \mathrm{Re}[Ae^{j2\pi m/M}e^{j2\pi f_c t}] \quad (3a)$$

$$s(t)=A\cos(2\pi f_c t+2\pi m/M) \quad (3b)$$

$$s(t)=A[\cos(2\pi mM)\cos(2\pi f_c t)-\sin(2\pi m/M)\sin(2\pi f_c t)] \quad (3c)$$

m=0, 2, …, M-1

Where A is the amplitude, f_c is the carrier frequency, $\theta_m=2\pi m/M$ are the M possible phase shifts of the carrier that convey the transmitted information, and M is a power of 2. $s(t)$ can be further reduced in terms if in-phase and quadrature-phase components to become

$$s(t) = A[I(m)\cos(2\pi f_c t) + Q(m)\sin(2\pi f_c t)] \quad (4)$$

where

$$I(m) = \cos(2\pi m/M) \quad (5a)$$

$$Q(m) = -\sin(2\pi mM) \quad (5b)$$

In case of imbalance the values of I and Q of eq (5) can be used in eq (1) to get I' and Q' for the imbalanced MPSK signal as

$$I' = (1+\varepsilon)\cos(2\pi m/M + \Delta\phi/2) \quad (6a)$$

$$Q' = (\varepsilon-1)\sin(2\pi m/M + \Delta\phi/2)I \quad (6b)$$

It is clear that if ε and $\Delta\phi$ are equal to zero, eq (6) reduces to (5)
It is common to represents the digital quadrature modulated signals by their signal space diagram. For the MPSK signals the signal space diagram is as shown in Fig. 1
It is clear from these diagrams that the possible symbol values are located on a circle whose radius represents the amplitude of the modulated signal A. This is expected since the transmitted information is represented by phase shifts only. Therefore, it is possible to assume that the MPSK signal has a unity amplitude for simplicity without any loss of generality i.e. A=1. In case of imbalance the effect is reflected on the constellation as shown in Fig. 2

Figure 3 shows a typical IQ modulator where the carrier signal and its quadrature each are multiplied by an appropriate weight according to the modulating symbols and summing the results. The imbalance effect is usually produced due to inaccuracies in the analog blocks of this modulator which are:

1- The digital to analog converter (DAC)
2- The two multipliers
3- The summator
4- The -90^o phase shifter

The resulting imbalance will affect the position of the transmitted symbols on the signal space diagram and this would lead to increase of probability of detection error.

In this paper a different technique is used to generate the MPSK signal using simple logic circuits to eliminate the need of analog circuits in the MPSK modulator. This way it is possible to avoid inaccuracies that causing a distorted signal space diagram.

THEORETICAL BACKGROUND

It is known from elementary mathematics that the n-order equation

$$z^n=1 \quad (7)$$

has n complex roots, and these roots are given by

$$z_i=e^{j2\pi(i-1)/n}, \quad i=1,2, \quad , n \quad (8)$$

and if n=M=2^k i.e. M is a power of 2, the roots of the equation

$$z^M=1 \quad (9)$$

can be found by repeated square rooting of 1. This can be expressed mathematically in this way

$$z^M = z^{2^k} = z^{(2)2^{(k-1)}} = (z^{2^{(k-1)}})^2 = 1 \quad (10)$$

If we make the change of variables

$$z_1 = z^{2^{(k-1)}} \quad (11)$$

Equation (10) will be reduced to

$$z_1^{\,2} = 1 \tag{12}$$

which is a second degree equation that has two roots. Before proceeding, it is useful to refer to the solution of the complex equation given by

$$z^2 = z_0 \tag{13}$$

where z_0 is a complex number. The solution of eq (13) is given by

$$z = \pm\sqrt{|z_0|}e^{j\theta/2} \tag{14a}$$

Where $|z_0|$ and θ are the magnitude and angle of z_0. Since the minus sign means a shift of angle of π radians, it is possible to write the roots in the form

$$z = \sqrt{|z_0|}e^{j\theta/2},\ z = \sqrt{|z_0|}e^{j(\theta/2+\pi)} \tag{14b}$$

Now, using the result of eq (14b) and the fact that z_0=1 in eq (10), it is possible to write the roots of eq (12) as

$$z_{11} = 1 = e^{j0},\ z_{12} = -1 = e^{j\pi} \tag{15}$$

Here, the first index represents the step of order reduction and the second index is the root index of that step. Following the same procedure, we will find that

$$z_2^{\,2} = z_1 \tag{16}$$

Equation (16) is actually two equations of the second degree because z_1 has two values (z_{11} and z_{12}), therefore, it will give us 4 roots (2 for each equation). Using the results of eq (15) and eq (14b), the roots of eq (16) will be

$$z_{21} = e^{j0},\ z_{22} = e^{j\pi/2},\ z_{23} = e^{j\pi},\ z_{24} = e^{j3\pi/2}$$

Since each step gives twice as many roots as the previous step, repeating this procedure for k steps will result in 2^k roots which are the desired roots of (9). These roots can be generally expressed as

$$z_{km} = e^{j2\pi(m-1)/M} \tag{17}$$

m=1, 2, …, M

Now, the similarity can be seen between the result of eq (17) and the general expression of the MPSK signal in (1c). Locating the roots given by eq (17) on the complex plane will make the same signal space diagram shown in Fig. 1.

In words, eq (17) is telling us that repeated square rooting of unity yields M complex phasors of M-level MPSK signal. The intention of this paper is to realize the root generation algorithm of unity described above by hardware circuits as will be explained in the next section.

GENERATION OF M-PHASE SHIFTS CARRIERS

Assuming that the amplitude is unity, the square rooting operation is basically a phase division by 2. This can be accomplished using the flip-flop (FF) because the FF does not only divide the frequency by 2, also the phase is divided by 2 as will be explained shortly.

For the purpose of explanation, the generation of 8-level PSK is demonstrated now. The circuit is shown in Fig. 4 where a high frequency clock with frequency f_0 is applied to a JK-FF, with the J and K inputs are connected to logic 1 so that the FF works as a T-FF. The outputs Q and Q' (where Q' is the complement of Q) are denoted as Q_{11} and Q_{12} and used as clocks to a second stage two FF's with outputs Q_{21}, Q_{22}, Q_{23} and Q_{24}, notice the similarity between subscripts notation of the outputs and the subscripts notation of the roots in the previous section, where the first subscripts denotes the stage and the second denotes the position of the output in that stage. The waveforms of the circuit are illustrated in Fig. 5.

Now, assuming that all FF's are initially set to low and that the FF's are negative edge triggered, then the outputs Q_{11} and Q_{12} will change at every high-to-low transition of the high frequency clock, with Q_{12} as the complement of Q_{11}. Now the FF_{11} with Q_{11} as input will have its outputs Q_{21} and Q_{23} change at the high-to-low transition of Q_{11} with Q_{23} as the complement of Q_{21}, at the same instance FF_{12} (with input Q_{12}) will have its outputs Q_{22} and Q_{24} undergo no change because its input Q_{12} is making a low-to-high transition. After a half cycle of Q_{11} and Q_{12} the situation is reversed, Q_{11} will have a low-to high transition at clock input, so no change in Q_{21} and Q_{23} while Q_{12} will have a high-to-low transition so the outputs Q_{22} and Q_{24} will change. Proceeding

in the same manner of analysis, the outputs of higher stages can be worked out as shown in Fig. 5. This arrangement of FF's is so much like the ripple counter except that the two outputs of each FF are used to derive two other FF's. This makes the circuit grows like a binary tree. Because of this similarity, the circuit will be referred to as the Multi-Phase Ripple Counter and denoted to as MPRC throughout this paper.

Assuming that the clock frequency is f_0, and looking at the outputs Q_{11} and Q_{12}, it can be seen that they have the same frequency $f_1=f_0/2$ and the two outputs are 180^o out of phase. While Q_{21}, Q_{22}, Q_{23} and Q_{24}, have the same frequency $f_2=f_1/2=f_0/4$ with ¼ cycle time phase shift between each other which is equivalent to 90^o phase shift, and for stage 3 $f_3=f_2/2=f_0/8$ with 1/8 cycle time phase shift.

This can be generalized by expressing the frequency and phase shift of waveforms of each stage by

$$f_n = \frac{f_0}{2^n} \tag{18}$$

$$T_{shift} = \frac{T_n}{2^n} \tag{19}$$

$$\theta_{shift} = \frac{2\pi}{2^n} \tag{20}$$

Where f_n and T_n are the frequency and the cycle time of the outputs of the n^{th} stage, and T_{shift} and θ_{shift} are the lowest time and phase shift between any two different output signals. Notice that all the possible phase shifts between any two output signals can be expressed as a multiple of θ_{shift}, in other words, if we take one signal S_0 as a reference signal with zero phase shift $\theta_0=0$, the phases of the signals of the n^{th} stage can be expressed as

$$\theta_m = (m-1)\frac{2\pi}{M} \tag{21}$$

Where, $M=2^n$ and $m=1, 2, 3, \ldots..2^n$

Which is the exact result required to be achieved

PROPOSED SYSTEM

Now to produce the MPSK signal, the generated waveforms can be multiplexed to one output by the data and the multiplexer output is filtered to be converted into sinusoidal wave. The filtering stage can be made in the power stage so that high efficiency class D amplifiers particularly current switching or current mode class D amplifiers (CMCD) [8] can be used in the transmitter since such modulator is suitable for constant amplitude modulations. Figure 6 shows a block diagram for the proposed MPSK modulator, where a high frequency clock of frequency f_0 is applied to the MPRC to generate M carriers each with frequency f_0/M and having phase shifts given by eq. (21). These carriers are then applied to an M-lines multiplexer, the select lines of the multiplexer are controlled by the modulating data so that each data code selects one carrier of a particular phase. The fact that these carriers have a frequency value equal to f_0/M and the value of f_0 is already limited by the implementation technology this means that the carrier frequency may not be chosen as desired, in such case, a heterodyne configuration of the modulator where a mixer stage can be used to adjust the carrier frequency as required.

IMPLEMENTATION OF TESTING AND MEASUREMENT SYSTEM

This technique is introduced as an alternative to the IQ modulator to generate MPSK signal to eliminate the IQ imbalance. Regarding the amplitude, the digital multiplexing of the different carriers into one output ensures the elimination of the imbalance in the amplitude. Regarding the phase, the different values of propagation delay of each FF can introduce phase imbalance because each carrier has a different path and hence may encounter a different delay.

An experimental circuit was built using TTL components to practically produce an 8-PSK signal, the circuit schematic is shown in Fig. 7. The Ic of 7476 which is a dual JK FF was used to implement the MPRC and the 74151 was used as the 8-to-1 multiplexer. To simulate the data, 3 stages of the binary counter 7493 was used to down scale the frequency of one of the carriers to lower frequency to simulate the data rate, this ensures that the carrier frequency is an integer multiple of the data rate instead of having a different independent clock for the data. The output of the multiplexer was applied to a BPF and compared to a reference signal of the same frequency and the x-y plot of the oscilloscope was viewed as shown in Fig. 8 where, the 8 phase patterns can be seen as 8 different ellipses. This

measurement was made at carrier frequency equals to 160kHz.

To measure the phase error produced due to the different propagation delay, the oscilloscope observation is not suitable because the measurement is taken from the time scale which is considered as an analog measure that may not be an accurately reliable measurement. To make a digital measurement of time, the output of the multiplexer and one of its inputs (considered as a reference signal) are fed to a computer through the parallel port interface. An MS DOS based Turbo C program was run in MS DOS real mode to read these two signals and measure the time difference. This program is run under MS DOS operating system (OS) not under Windows OS because Windows is a multitask OS and it is not a convenient platform for timing critical programs because the processor time is shared among multitasks including the user's program which in turn would affect the time measurement task of the program.
The time measuring Program was tested for the highest sampling frequency possible (which is limited by the speed of the PC), the sampling frequency was found approximately 800 ksample/s. Although, this value of the sampling frequency seems rather high, but it is actually not. Since we are trying to measure time, we need to consider the minimum timing interval which is 1/8 of a cycle and to assign say 20 samples for 1/8 of a cycle, the frequency of the carrier should be

$(1/f_c)\times(1/8)=20\times 1/f_s$
$f_c = f_s /(8\times 20) =800/(8\times 20) = 5$ kHz

This means that the clock frequency should be $f_{clock}=8\times 5=40$ kHz. Although, the 5 kHz value as a carrier frequency is not practical, but it was chosen due to the limitations imposed by what was available of measurement tools that is the MS DOS based PC.
The basic idea of measuring the phase difference between the two signals is

1- Detect two successive low-to-high bit transitions of the first signal and calculate the number of samples in between as the time of one cycle.
2- Detect a low-to-high transition of the first signal and a low-to-high of the second signal and calculate the number of samples in between as the time shift.
3- Calculate phase = (time shift / cycle time) × 360

After measuring the phase difference between the output signal and the reference signal, the phase error was calculated as RMS value and the results were as in the table below
As can be seen from the above table that the phase deviation from ideal phase values is rather low, two important factors need to be considered when evaluating these results. The first factor is that the carrier frequency is low and it has been mentioned earlier that the imbalance parameters are in general frequency dependent and for higher frequency values it is expected that the situation is worse but on the other hand the fact that the measurement time is being quantized by the sampling period leads to the generation of certain amount of error that is added to the actual phase imbalance introduced by the circuit. The second factor is that the source of phase imbalance produced by this circuit is due to the different paths that different carriers take and hence different propagation delays are encountered. Theoretically if all paths have equal propagation delay, no phase imbalance will be introduced. In practical situation this is not the case, but the amount of difference in the propagation delays is an implementation technology dependent and the circuit was implemented using TTL technology (which is rather old technology) because of its availability at hand. It is expected that modern implementation technology will have better performance that the TTL technology, like [9]:

1- Dynamic Current Mode Logic (DyCML)
2- Gate-Diffusion Input (GDI)
3- Race Logic Architecture (RALA)

CONCLUSION

In this paper a new technique for generating MPSK signal is presented in which no analog components are used to generate the modulating phase shifts and hence eliminating or reducing the amplitude and phase imbalance. A practical circuit was built using TTL components to generate an 8PSK signal and the results was presented as the 8 ellipses for 8 phase differences, also the time measurements was made for lower frequencies to measure the phase imbalance.

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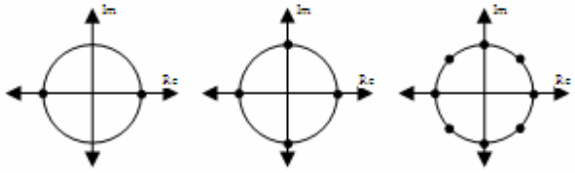
Table (1) The measured RMS phase error

Ideal Phase difference in degrees	Respective RMS of phase error in degrees
0	0.00
1/8 × 360	0.57
2/8 × 360	1.14
3/8 × 360	0.58
4/8 × 360	1.13
5/8 × 360	0.57
6/8 × 360	1.14
7/8 × 360	0.57



(a) (b)

Fig. 1 Signal space diagrams for MPSK signals with (a) M=2, (b) M=4 and (c) M=8.

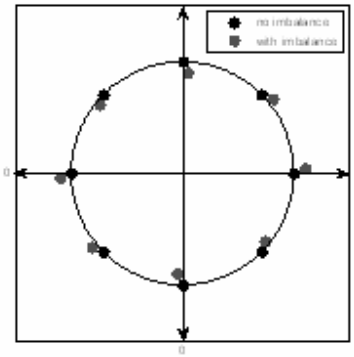


Fig. 2 8PSK constellation with imbalance (ε=0.1, $\Delta\phi$=5°) without and imbalance.

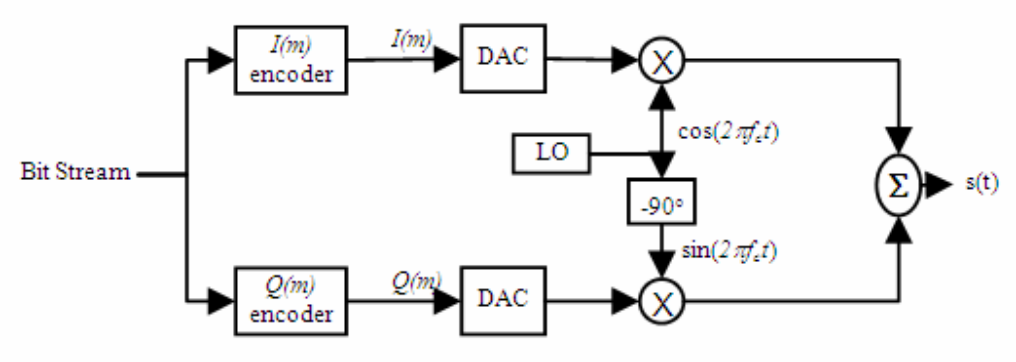


Fig. 3 A typical MPSK modulator.

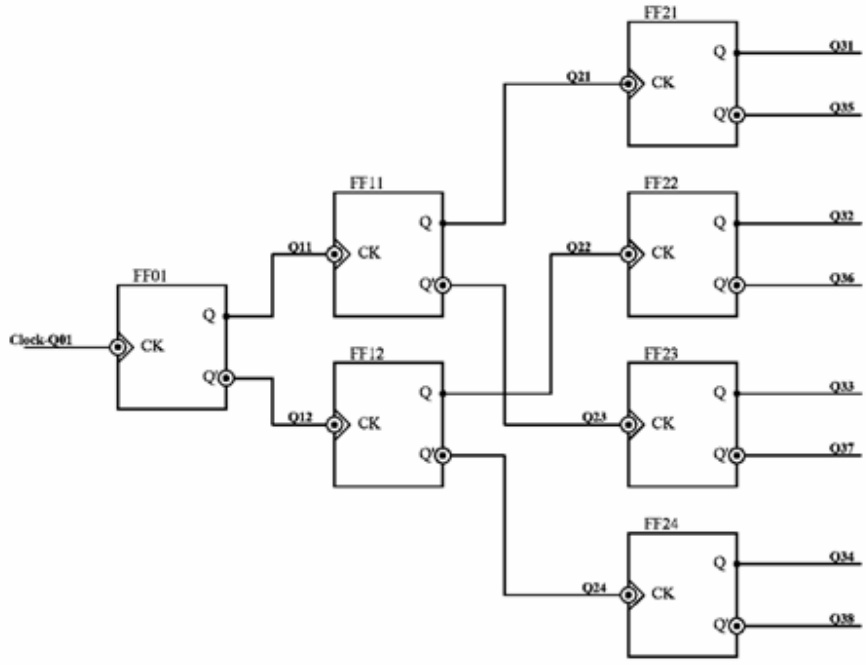


Fig. 4 Multi phase ripple counter.

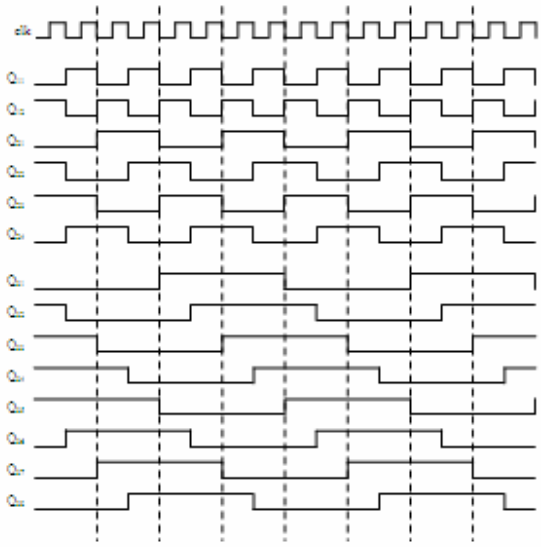


Fig. 5 The waveforms generated by the MPRC

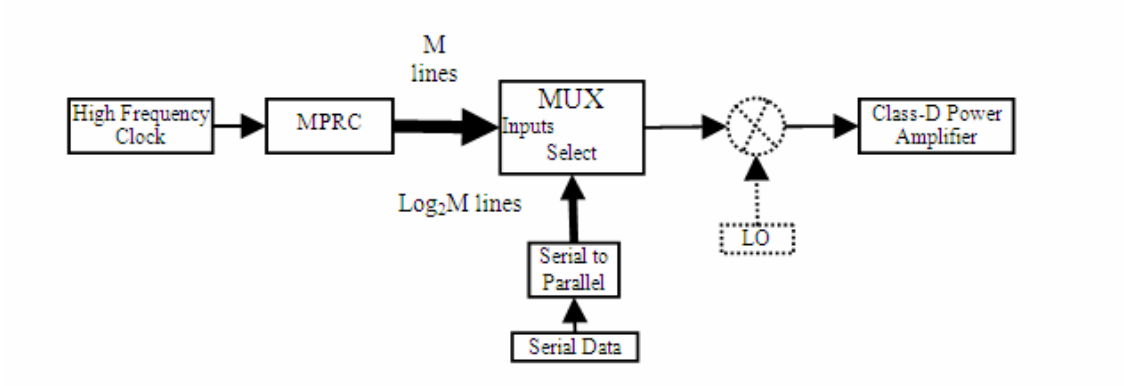


Fig. 6 The proposed system for MPSK transmitter

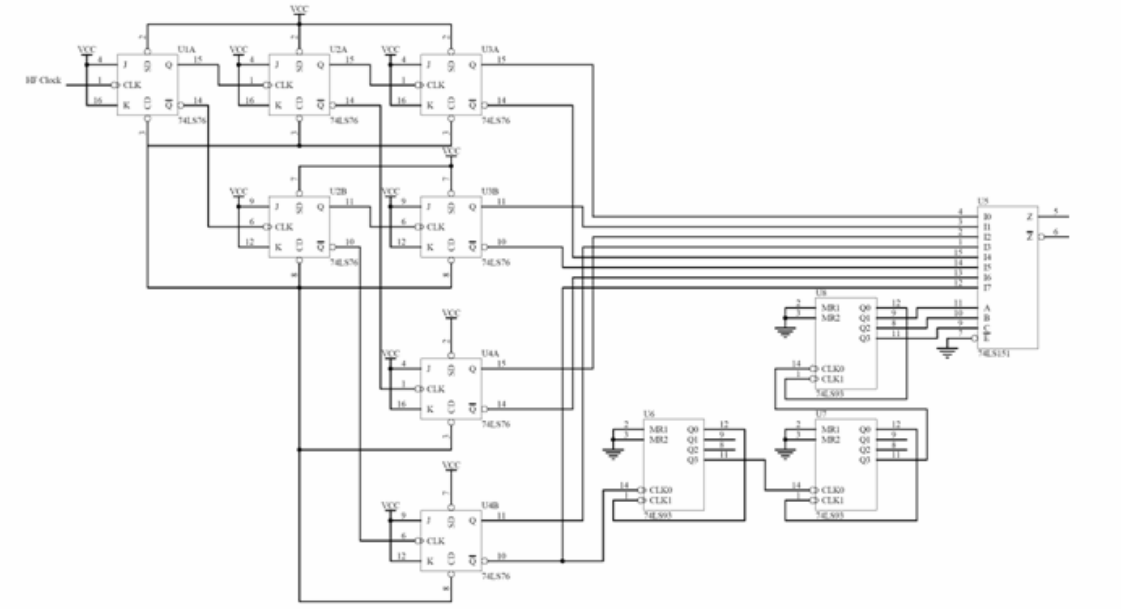


Fig. 7 The test circuit for generating the 8PSK signal.

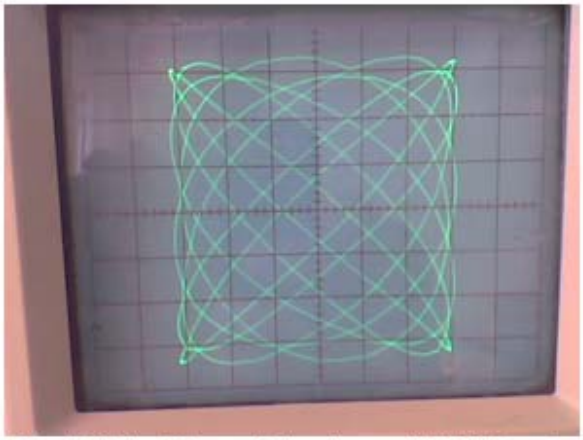


Fig. 8 Eight ellipses of the phases of 8PSK signal.