DESIGN AND IMPLELMENTATION A PC BASED SYSTEM FOR CIRCUIT TESTING

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ABSTRACT

This thesis deals with design and implementation of PC based control unit for testing systems. The design of the system involves mainly the hardware circuits, and software.
The tester carries out the following types of test Analog circuit test, Digital I.C. test, In-circuit test, and functional test.
The system designed and implemented, the implemented system hardware was built around two parallel ports. The hardware includes four buffers used as I\O channels addressed as Analog input (A\I), Analog output (A\O), Digital input (D\I), and Digital output (D\O). The system also includes Analog to digital converter, Digital to analog converter, and resistor testing circuit. The data to processed can be in digital or in an analog form. In the same time the hardware outputs controlling signals for testing and controlling the equipments. These signals are in digital or analog form.
The implemented system software has two main user interfaces, one for selecting the mode of operation (as read or write), and activates the associated buffer. The other which included the functions of tests.
For the resistor testing, I.C. testing, and circuit testing the system software compares inputs from the unit under test (UUT) with stored upper and lower limits, if the input is a value between them the test is considered successful otherwise the test fails.
The software has been written in "Visual Basic" programming language running under windows® (ME\XP) operating system environment and tested on the already exist hardware.
The system has been tested and it worked successfully for different resistance value and different types of Digital I.C.

INTRODUCTION

The manufactures of the Printed Circuit Board (PCB) face the constant challenge of determining the quality of the product they build. All manufactures have to inspect finished products to insure that they satisfy the required quality standard [1]. Electrical testing has always been an essential tool used in these determinations [2].
A general definition of a test is an experiment done either to confirm or deny a hypotheses or to differentiate between two hypotheses. Testing a device means checking it whether it is operating as expected or not. In any type of testing, needed to know two things. First, which input stimuli should be applied to the device? Inputs should apply only those inputs
that activate the fault i.e. the inputs which result in different outputs from the

The need for more effective methods has long been accepted as common place among electronic engineers [3].
The idea of having test equipment, which can check the components in circuit, to determine its performance is an attractive work [4].
Different testing techniques are needed to test the whole board. Automatic testing of electronic devices has been a major factor not only in the overall improvement of product quality and reliability, but also in the dramatic lowering of product costs [3].

Types of Testing Approaches [5].
There are some basic approaches for testing populated circuit boards or modules. These are:

Functional Testing: Using this approach, a board is inserted into an actual system and its behavior is observed while the system performs its regular functions. This approach has several major shortcomings. First, it is extremely difficult to diagnose a failure. Second, it is difficult to develop complete test suites, or even measure how good a given test suite is. In general, it is extremely difficult to develop quantification of faults (or defects) that are covered by a given functional test. This is because no algebra that defines and links functional activity to physical defects such as shorts or opens among the nets. Ones tests are developed; there isn't any mathematical method for determining fault coverage. Only "guesstimates" are available. Finally, functional test set up may be very costly since it is unique to each different board and may also require ancillary functions (e.g. disk unit, etc.) to be available functioning in order for Unit Under Test (UUT) board to be tested.

Card-edge Testing: This is different Testing approach when compared to one above. In this case, a "card-edge"(i.e. edge connector) tester is used to insert UUT board in order to apply signals sequence/combination of signals (and observe responses at all times) at the card-edge. Thus, whereas the card-edge tester can be programmed to mimic the exact behavior of the target system for the UUT board it can also be programmed to control and observe the signal values along the edge-connector at a fine resolution. This improves the testability of the UUT but, like the Functional Testing approach, difficulties in test generation and coverage assessment remain very high. It also suffers from limited-access since complex boards, nets and components on the "interior" of the PCB are difficult to test due to limited access from just the edge connector.

In-Circuit Testing: ICT was developed in response to difficulties in creating card-edge and functional tests in the late '70' and early 80's. This technique represents a major departure from the Functional Testing (and card-edge testing) approach, in that it tests one component on a PCB at a time. As the PCB's functional complexity grew, it became difficult for engineers to understand the entire PCB functionality and test generating tools had difficulty in crating tests for the entire PCB. The 'one IC' at a time became a convenient divide-and-conquer approach to minimize test development time by breaking down the PCB into small MSI (at that time) circuits such as an AND gate that tests could easily and automatically developed. To achieve its goal, In-circuit Testing (ICT) uses a bed-of-nails fixture to contact the board-level nets in order to apply electrical stimulus and observe the response. The bed-of-nails fixture provides an array of spring-loaded test pins that come into contact with the UUT board at specifically designed points, called test points, whose locations must be planned during board layout so that there is sufficient surface area and clearance for paper contact to be made at each pin position. Each test point may be used to inject a signal value into the corresponding net or to observe its present value.

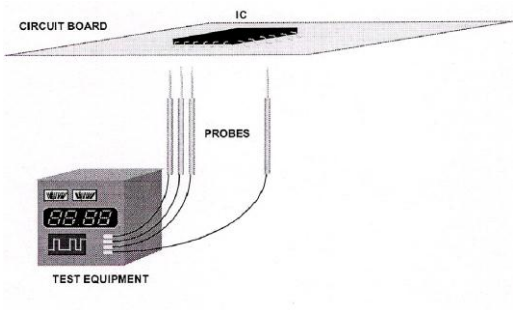


Fig1. Illustration of In-circuit Testing

1.2 Related Works

In 1979 Schreiber made the first Automatic Test Generation Technique classification. But it was in 1979 when P.Duhamel and J.C.Rault published a more exhaustive categorization of known analog circuit testing methods. The types of tests and faults to diagnose were given and classified. The methods were grouped into estimation techniques, topological methods, taxonomical methods and methods for linear circuits [10].

In 1985 J.W. Bandler and A.E. Salama reported another excellent classification, including methods that had just appeared and improvements obtained from them. This is one of the most referenced reviews for analog electronic circuit testing. They classify the methods into two main groups: techniques that need a simulation before the test, and the ones that need the simulation after the test [7].

In 1987 Mohammad Baha Al-Deen used a microcomputer as a based system for circuit testing. The project used the microcomputer as a part of an automatic test system used for Analog In-circuit PCB testing. Testing operation were achieved by comparing voltage taken from UUT with data stored in the microcomputer and the results were displayed by using monitor or a printer to printed out the results [4].

In 1999 Malathe AL-Qezweeny used also a microcomputer in design and implementation a telephone tester. The project used a computer (NEC6001) as a dedicated computer based automatic telephone tester suitable for testing push button and rotary telephone sets [9].

In 2002 Waseem AL-Haidari used a personal computer to build a data acquisition and monitoring system for (Automated Test Equipments) ATE. The system used Industry Standard Architecture (ISA) bus to interface with testing circuit [9].

2. BASIC CONCEPTES OF TESTING SYSTEMS.

The problems associated with testing have increased with introduction of each new generation of equipment. An important contribution towards solving these problems has been made by the introduction of automatic test methods [3].

2.1 Type of Faults: Test Capabilities and Selection

The process of testing or diagnosing circuits consists in applying certain types of excitation to a circuit and then analyzing the responses obtained in order to derive a possible failure. A fault could be defined as any variation of a component value from the nominal. This could produce an abnormal behavior of the global circuit [8]. A typical Automatic Test Equipment (ATE) environment is the one shown in Figure 2

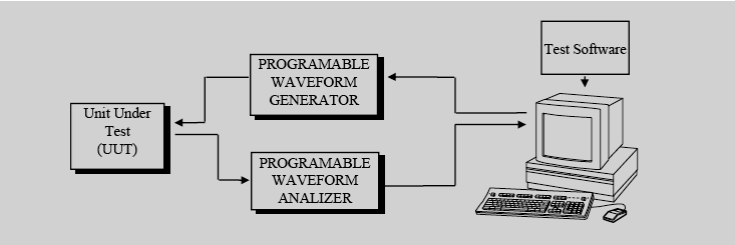


Fig2. : Basic structure of an ATE system

According to the figure, an ATE system should carry out the following basic actions: [10]

. Signal generation, using an external device such as an acquisition card DSP board, waveform generator operated via a GPIB bus, etc. It is necessary to have a set of stored input signals that produce particular circuit responses that are useful for fault detection and isolation. These input stimuli could be sine waves, square waves, DC-signals, ramps, etc.
Take measures from the circuit and obtain signatures. The output response can be interpreted in time or frequency domains. Once the measures are taken , some features can be extracted, for example a tuple [overshoot, rise time] or a particular sequence corresponding to the signal shape. The set of parameters that characterized a signal is known as a signature.

3. Interpretation of the obtained signatures. These signatures can be compared with the ones previously stored, or used to derive possible parameter values. These tasks require an appropriate diagnosis strategy.

There are many researches in the bibliography concerning the testing or diagnosing of electronic circuits. The objective of these two disciplines is almost the same but, although they have a lot in common, there is an important difference between them. In general, the purpose of the test , as it is known in the industrial domain, is to detect a fault in a circuit, while fault diagnosis is not only to detect but also locate the fault or fault identify the incorrect parameter values [10]. Both domains are described in the following paragraphs.

2.2 Functional testing and In-circuit testing

Printed circuit board testing can be divided into two different approaches, namely In-circuit testing and functional testing. Each has a specific job and solves a specific problem.[4]

In-circuit testing can be considered as a diagnostic tool, While functional testing tests the characteristics of parts, electronic performance of the circuit and determines whether a PCB is a fault-free or not. [11]

2.3 The concept of in-circuit tester operation

The testing theory of an in-circuit tester is based on comparison With known good unit. Good master unit (such as: component, circuit, IC, etc) are measured in predetermined sequence and the obtained data are stored in the memory of the computer. The unit to be tested is measured in the same sequence to see if the measured values lie in the certain range centered around the stored data samples. The unit under test is judged to be good if the measured values are the same as the data samples or lie in the certain range centered around them, Therefore the accuracy of the samples is an important point in deciding the performance of the tester.

2.4 Guarding Technique

As mentioned previously, in-circuit testing involves tests of individual components mounted on a PCB, hence the major task of an in-circuit tester is to exclude the influence of other components surrounding the component under test, and this can be achieved using guarding technique.

Guarding is a technique to eliminate as much as possible the effect of impedances surrounding the component under test in order to measure the actual value of the component. Without guarding, the percentage of components showing a value almost equal with the actual value is 50 to 60 percent for analogue boards and about 80 percent for digital boards [12]. However, these rates do vary according to the kind of the circuit.

The guarding technique uses the characteristics of an op-amp for isolating the component under test from the effect of parallel impedance caused by other components. A typical situation is shown in a Fig. (3) with Rf is a known feedback resistance and Rx is the resistance to be measured, when the measuring voltage Vi is applied, Vo is generated as determined by:

$Vo = - (Rf / Rx) Vi$

Since the non-inverting input of the op-amp in fig. (3.) is grounded; hence, it is at zero potential because of the virtual short. As a result of both ends of R2 comes to zero and current would flow through it. The current through R1 flows to ground and return to the input voltage source Vi, hence the output voltage of op-amp will be proportional to the value of Rx only (since Vi and Rf are constants).

Generally speaking, when impedance Zx on a circuit is under the influence of parallel impedance caused by several other components, it is possible to eliminate the influence of other components and measure Zx, with one end of all other components grounded.

It should be noted that the guarding technique is not applicable to cases where there are two or more individual components completely in parallel. In such instances, the in-circuit tester views theses parallel components as a single component with an impedance value equivalent to the impedance formed from the parallel combination. This is a limitation of all in-circuit testers.

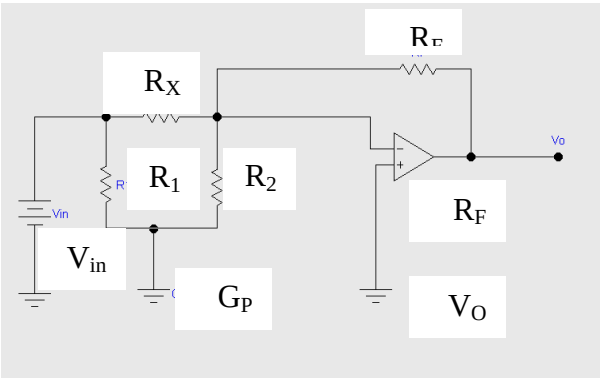


Fig 3. Testing guarded resistor

Digital IC. Testing

The evaluation of the reliability and quality of a digital IC is commonly called "testing", yet it is comprised of distinct phases which are mostly kept separate both in the research community and in industrial practice.

Verification [13]

This is the initial phase in which the first prototype chips are "tested" to ensure that they match their functional specification, that is, to verify the correctness of the design. Verification checks that all design rules are adhered to, from layout to electrical parameters; more generally, this type of functional testing checks that the circuit: (a) implements what it is supposed to do and (b) does not do what it is not supposed to do. Both conditions are necessary. This type of evaluation is done at the design stage and uses a variety of techniques, including logic verification with the use of

hardware description languages, full functional simulation, and generation of functional test vectors. Figure (4) shows the principles of testing digital IC.[14]

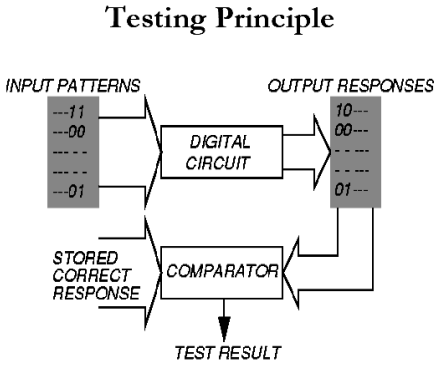


Fig 4. Testing Digital IC. Scheme.

Test Pattern Generation [13]

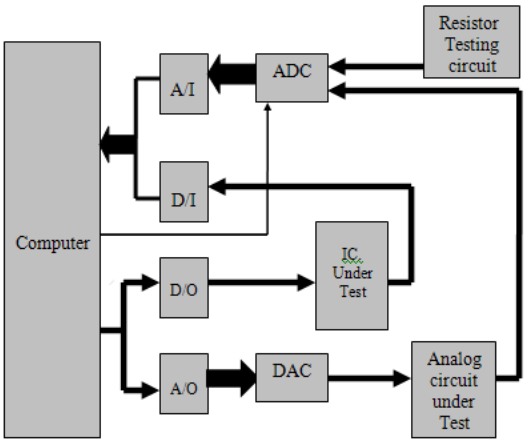
Test pattern generation is the process of generating a (minimal) set of input patterns to stimulate the inputs of a circuit, such that detectable faults can be exercised (if present) . The process can be divided in two distinct phases: (a) derivation of a test, (b) application of a test. For (a), one must first select appropriate models for the circuit (gate or transistor level) and for faults; one must construct the test such that the output signal from a faulty circuit is different from that of a good circuit. This can be computationally very expensive, but one must remember that the process is done only once at the end of the design stage. The generation of a test set can be obtained either by manual methods, or by algorithmic methods (with or without heuristics), or by pseudo random methods. On the other hand, for (b), a test is subsequently applied many times to each integrated circuit and thus must be efficient both in space (storage requirements for the patterns) and in time. Often such a set is not minimal,

3. HARDWARE IMPLEMENTATION

The implemented system is used to test analog passive components (resistors), analog voltages, Digital IC and resistance potential divider. The system is based on using a computer. The test results are displayed on the screen of the RGB monitor.

The block diagram of the testing system is shown in the figure (5) the system consists of several connected units, and consists of the following main units.

Input/output interface unit.
Analog to digital conversion unit.
Resistor testing unit.
Digital IC testing unit.
Digital to analog conversion unit.
Functional testing unit.



Each of these units will be described in details.

Fig(5). Block diagram of the Testing System.

3.1 Input/output interface unit

Interfacing is a term that is applied across a broad range of electronic implementations. It relates to systems as well as to individual components. Interfacing usually involves effectively traversing a boundary one entity to another. In the field of electronics, the entities can be viewed in a hierarchical fashion from a system, subsystem, components.

The tester is interfaced to the computer system via a parallel port. The tester uses the four 74245 octal buffer line drivers (bi-directional buffer) to interface to the computer system. This device is used for several good reasons; it buffers the computer port during the communication with external hardware.

A more important function of these devices is that of computer protection. The devices help to isolate the computer bus from outside problems.If the external hardware were tied directly to the computer bus, this protection would be missing.

The 74245 has the DIR pin to select the direction of data transfer, so this pin is put logic 1 or 0 depending on the direction selected from side A to side B, or from side B to side A respectively. The four buffers can be used as follows depending on the DIR pin. Analog input (A/I), Analog output (A/O), Digital input (D/I) and Digital output (D/O).

In the proposed system two parallel ports can be used as LPT1 and LPT2,

Figure (6) represents the circuit diagram of the input/output interface unit. The 8-bit data group of the LPT1 is connected to the A data port of the four 74245. While 4-bit of the data group of LPT2 are connected to the Output Enable OE pin of the four buffers respectively.

The aim of this connection is to switch between the buffers by sending an appropriate set of word that activate one of the buffers and isolate the others.

There are another 3-bit from the data group of the LPT2 are connected to the status group of the LPT1 to indicate it to set the 8-bit data group in read or write state to match with the active buffer.

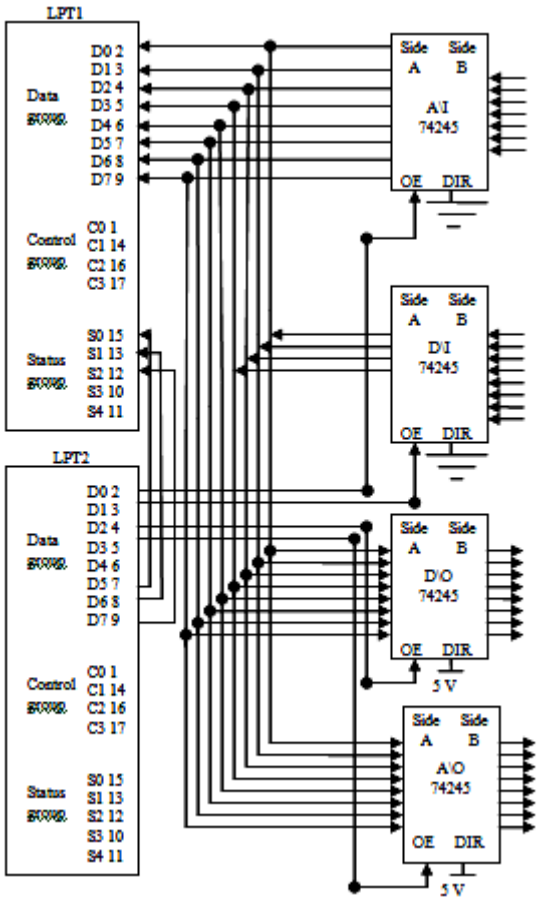


Fig 6. Circuit Diagram of I\O Interface unit

3.2 Single chip data acquisition system (Analog Multiplexer/ADC)

An analog multiplexer is simply a switching unit having a number of analog input channels and a single output channel, which is connected in turn to each of the individual input channels. So the output is one of the inputs and the selection of which one of the inputs will appear at the output is under digital control like a simple decoder. The input to the decoder represents the address of analog input channel and the number of the line inputs to the decoder depends on the number of analog inputs to the multiplexer. In the proposed system three lines from LPT1 are input to the decoder to select one of the 8-chaanels.

The analog Mux is used to couple the output of the test circuits to the ADC in a preset sequence, while the ADC is used to convert these output analog signals to their digital equivalent by comparing it against a reference signal. In the proposed system the ADC0816 is uses a Successive-approximation technique, which is a feedback system operates on a trial and error technique to approximate an analog input with the corresponding digital code. figure (7) shows the circuit diagram of ADC chip interfaced to the A/I buffer

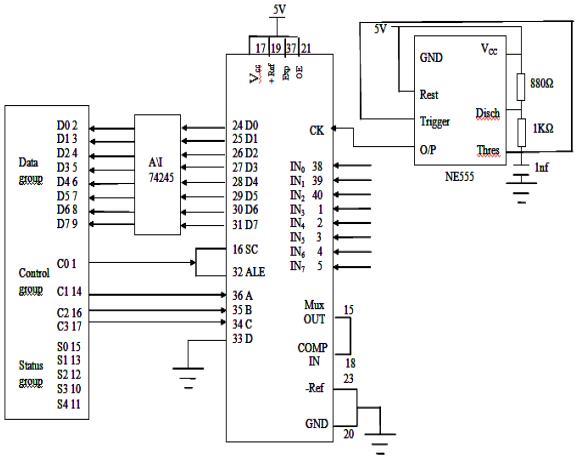


Fig 7. Circuit Diagram of ADC

- Test Circuit for resistors

The test circuits use an op-amp type (LM 358, App.A-3) as the basic building block.
Constant voltage technique is used to test the resistors. The range values of resistor testing circuit covered are between 100 Ω to 15 kΩ, these values are divided into two ranges:
Low range resistors (100 Ω to 1 kΩ).
High range resistors (2.2 KΩ to 15 kΩ).
Each range has a separate test circuit. Figure (8), shows the resistors test circuit. The difference between the low range test circuit and the high range test circuit is the feedback resistor (Rf).

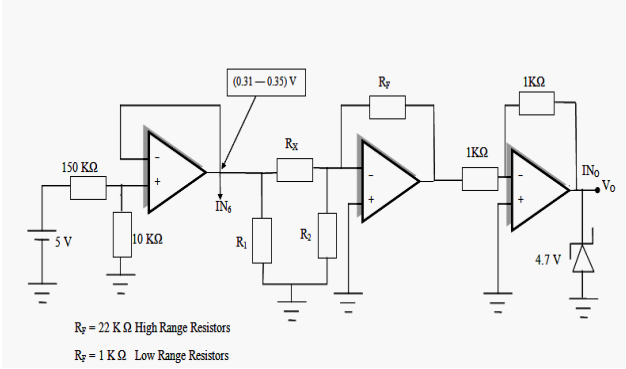


Fig 8. Test circuit for Resistors.

- Digital I.C. Test

One of the main functions that test system does is digital I.C. test. This system tests three types of digital I.C. 74LS00, 74LS08, and 74LS32.The test procedure can be described by three phases. Generation of an appropriate test bit pattern that produces a desired output, that will be done by software which writes the test bit pattern to parallel port (LPT1). This test pattern is applied to the I.C. under test through the D\O buffer which connected to Latch (74LS373, App.A-4). The purpose of using latch is to capture the test bit pattern and apply it to the I.C. under test when the D\O is off and D\I activated. The Enable of the latch and the Output Enable (OE) of the D\I are connected together. So at the beginning of the test D\O is active, D\I is off, and latch behaves as a buffer i.e. the output of the latch follow the input. The next step is to change the status of D\I to be active, in the same time the latch latched the last output. Finally the D\O is set in off mode. The last phase of the test procedure is reading the output response that's come from I.C. under test through D\I and parallel port (LPT1), and compares the output with truth table of the specific I.C. and display the result. Figure (9) shows the circuit diagram of the I.C. tester.

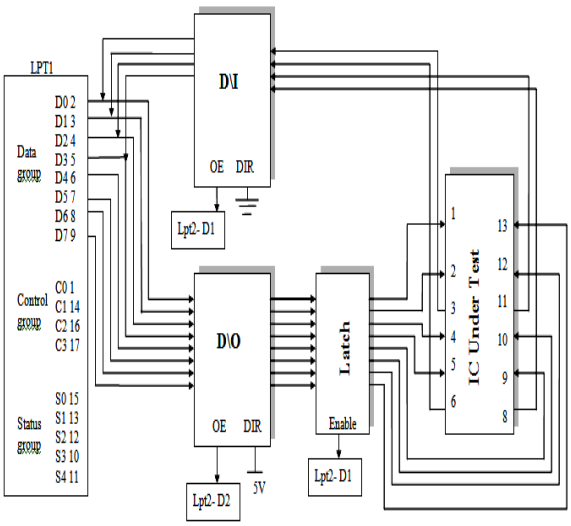


Fig 9. Circuit Diagram of I.C. Tester Circuit

- Testing Circuit Response

This type of test can be called Functional test. It depends on applying certain input on the circuit under test and compare the result obtained by the expected one. In this system an input signal generated from PC is applied through A\O buffer and is converted it into analog form by using digital to analog converter (DAC). The type of DAC used in this project is called R2R DAC, Figure (3.8) shows the circuit diagram of the DAC. The output of the DAC is connected to a buffering circuit to prevent any change in the value of the output of DAC because of load balancing. The output of the DAC is connected to ADC through channel three to check the value of voltages applied to circuit under test. The output obtained from the circuit (Attenuation circuit used in this project) is applied back to ADC through channel two. Figure (10) shows the circuit diagram of attenuation circuit.

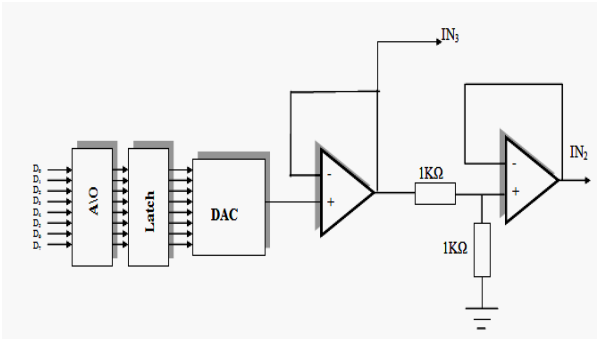


Fig 10. Circuit Diagram of Attenuation circuit

- RESULTS

4.1 User interface

The software of the system consists of two main user interfaces, one is used for choosing the type of operation as Digital input test, Digital output test, Digital I.C. test, and Analog test. Figure (11) shows the user interface according to parallel port 2

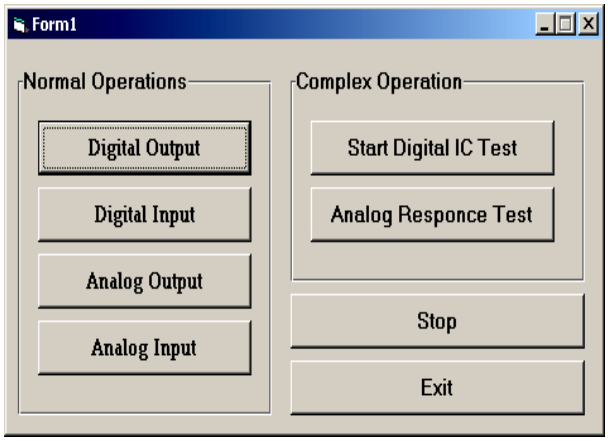


Fig11. User interface according to parallel port 2

The second one receives the order and displays the type of operation and contains the testing program function as receiving the settings and displays the results. Figure (12) shows the user interface according to parallel port 1.

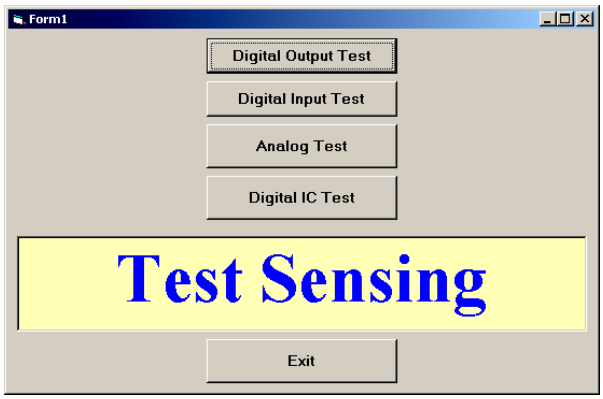


Fig 12. User interface according to parallel port 1

As mentioned previously when the operator clicks one of the button in Fig (11), the type of the clicked button immediately appeared in the text box in Fig (12).The message that appears in Figure (12) presents at the start of the program, which mean that LPT1 senses which mode of test sent to it from LPT2.

Digital I.C. test results

The first two steps is the same in each operation of any type of test, the choice of type and clicking the test button as shown in **Fig (13).**

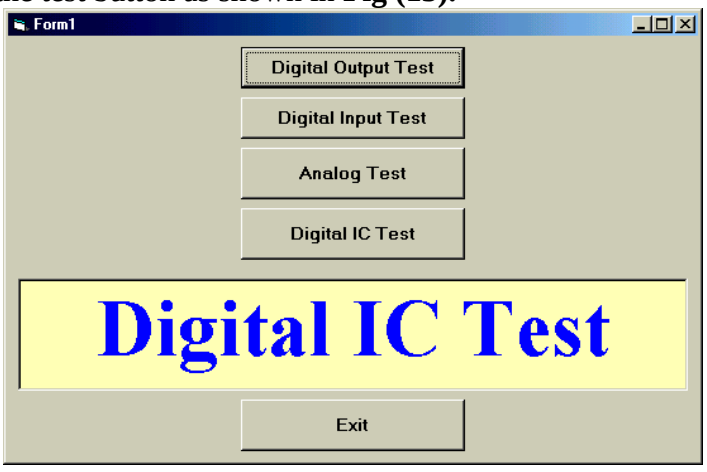


Fig 13. Selecting I.C. test

The operator will present with a new window that contains the type and number of I.C.s. He selects one of them for testing as shown in Figure (14).

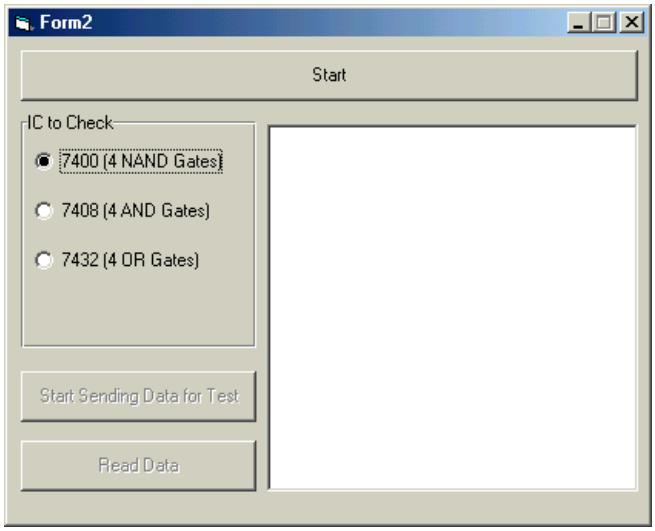


Fig14. Selecting I.C. under test

When the operator selects I.C. to be tested and then click start button the test starts and the result will be displayed, Figure (15), and Figure (16) shows the results obtained from testing two I.C.. One passed test and the other failed.

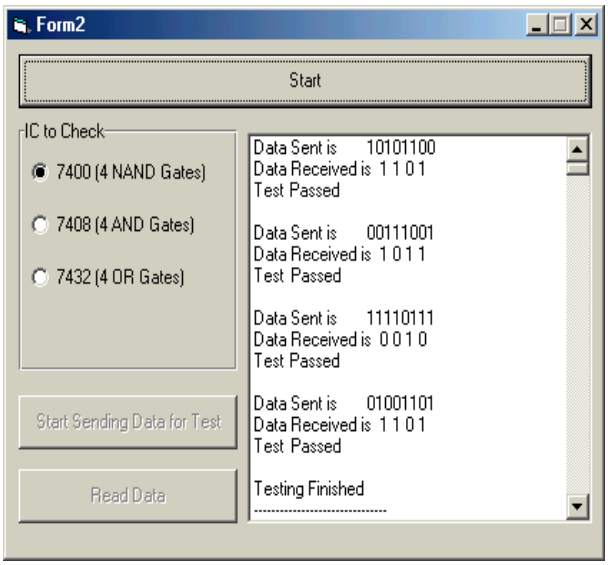


Fig 15. 7400 I.C. passing test result

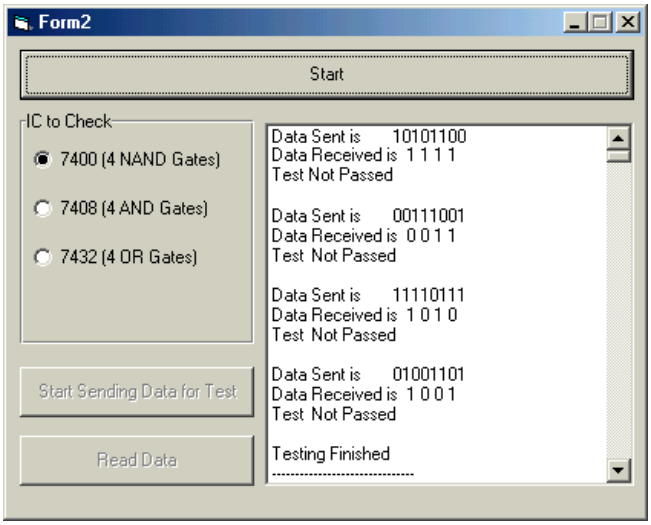


Fig16. 7400 I.C. Test is failed

After the test finished, a new window appears asking the operator to choose the next I.C. to be tested as shown in Figure (17).

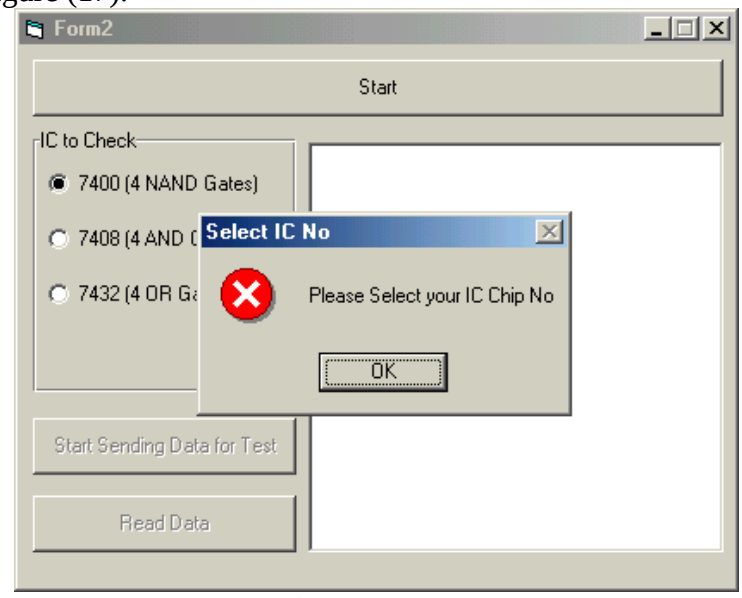
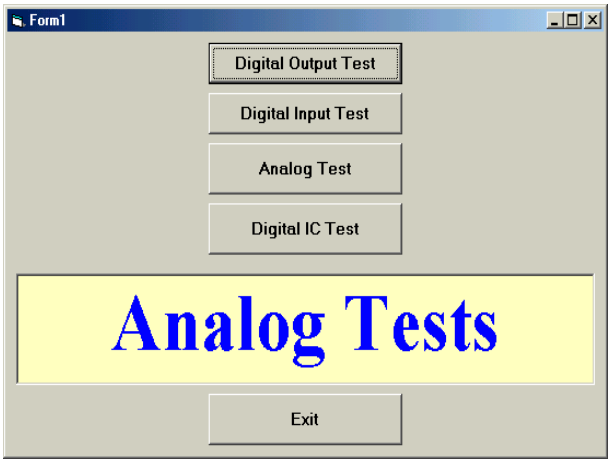


Fig 17. Selecting new I.C. to test

Analogue Test results

When the operator selects to test in analog mode. So at analog test message presents in text box, as shown in **fig (18):**



F**ig18**. Selecting Analog test mode
The operator after clicked the analog test button in Fig (18), a new window appears. Figure (19) then displays set of buttons each one of them indicates the type of test.

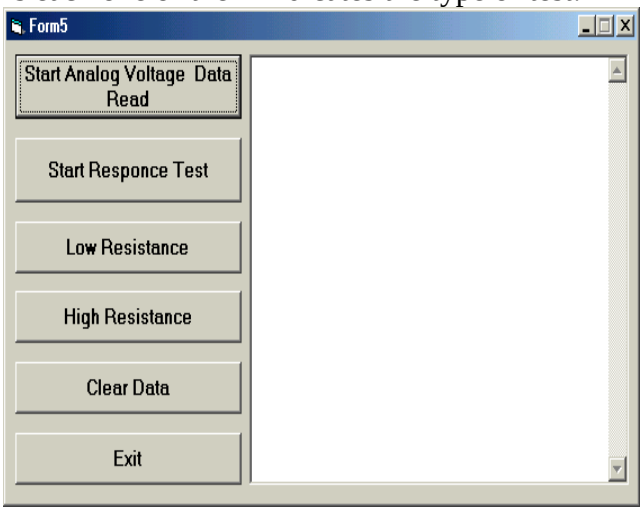


Fig 19. Analog test selection interface.

Analogue voltage results
This system displays the values of three different voltages and display the channel connected to it. Figure (20) displays two reading to the channels. In channel 6 there is different in the value because changing in the voltage.

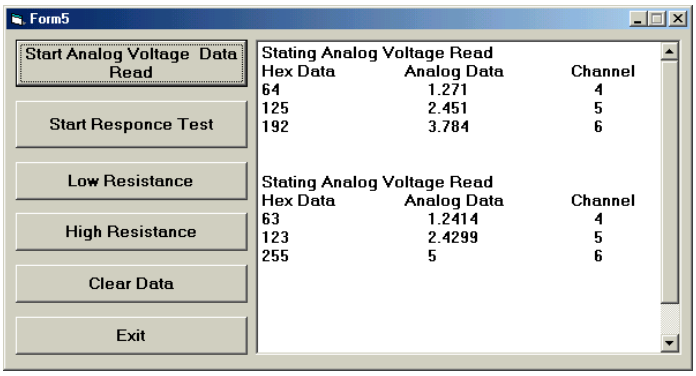


Fig 20. Analog voltage data read results

Response test results
The operator when clicks "Start Response Test" button the program presents a message showing to the operator the value of the voltage from DAC, also it shows the expected response of the attenuation circuit, and display the upper and lower acceptable limits. The program then displays the practical value of the response as read by the system and compare it with limits and finally displays the result as the circuit passed the test or failed. Figure (21).

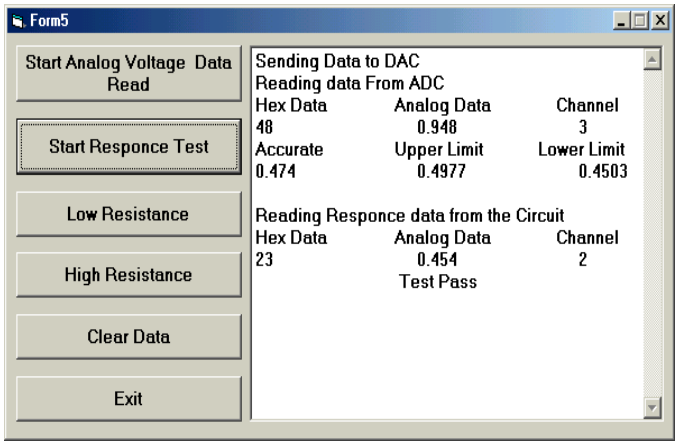


Fig 21. Circuit response result

Resistor test circuit results

The operator must first set the value of resistor to be tested and starts the test. The program then sets the upper and lower acceptable limits. Read the value of the voltages, calculate the resistor value, compare it with the limits, and display the result where the test pass or not. Figures (22), and (23) for low range.

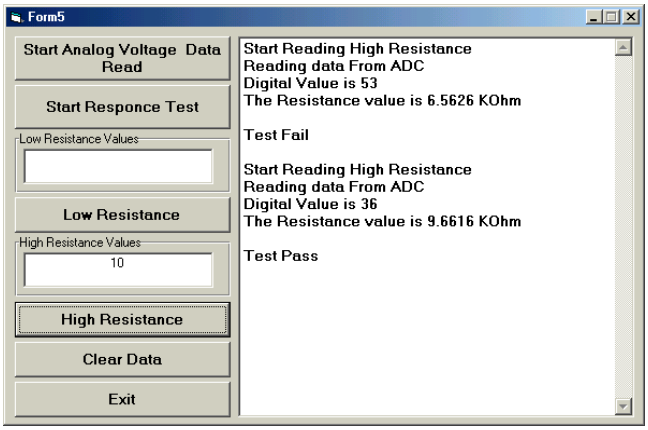


Fig22. High range results

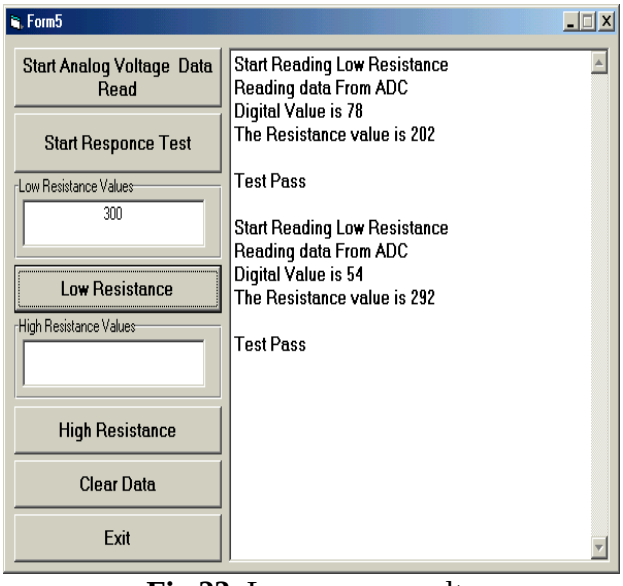


Fig 23. Low range results

Sources of errors

-. Deviation from the amplifiers ideal characteristics

The op-amps used in test circuits is considered to be ideal, in fact there is no ideal op-amp due to various types of non-idealness of the circuit performance, such as finite input impedance which allows a voltage drop to exist between the inverting terminal and the guarding point. To minimize this voltage drop, an op-amp with very high input impedance (MOS or bipolar-field effect (BIFET)) should be used to minimize this voltage drop.

-. Errors in the ADC

The system uses an 8-bit ADC. The bit resolution is 0.019V which represents the basic error introduced by the ADC. This value of bit resolution will affect the accuracy of conversion especially for low values of DC voltages. The ADC error was taken into account when determining the upper and lower limits.

-. Conclusions

In previous chapters, the design, implementation, and testing of a flexible a PC-based test system has been carried out.

In this work, Automatic testing system has been designed and implemented which consists of two parts: the hardware circuits and software programs. The hardware structure consists of two parallel ports, Buffering circuits, resistor testing circuit, latching buffers. The First parallel port used to transfer the bi-directional data, while the second one used for controlling the I\O buffers and signaling the first parallel port to which mode to is set. The four I\O buffers used for isolation of the parallel port and to switch between types of I\O so can be called it as A\I, D\I, D\O, and D\I. To indicate to Analog or Digital input or output. The ADC chosen for the design of analog input section is Monolithic I.C. (ADC0816), which is appropriate for low speed input signals.

The software design of the system consists of two main parts: Selecting of the type of test, and the performing of the test. The selector parts is used to activate one of the four I\O buffers and indicates the first parallel port to change it's mode from writing to reading depends on the indications. The second parts is responsible of performing each type of test as reading the values, making the calculations; comparing the results with the limits, taking the decision as pass the test or not, and finally displays the results. The upper and lower limits can be adjusted to meet any modification introduced, by simply changing the reference values stored in the computer.

The system software is implemented by using Visual Basic.6. The software structure of the Automatic test system algorithm is a general algorithm, which can be modified to achieve a specific function. The proposed system can be described as a prototype system which can be easily modified (by adding some function) to match the system under test.

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