# Design and Implementation of Single-Phase Boost PFC Converter

**Prof. Dr. Jafar H. Alwash,**
Department of Electrical Engineering
College of Engineering
Baghdad University
Email:jalwash@yahoo.com

**Asst. Prof. Dr. Turki K. Hassan,**
Department of Electrical Engineering
College of Engineering
Al-Mustansiriyah University
Email: turkihassan@yahoo.com

**Asst. Lect. Raed F. Abbas,**
Department of Electrical Engineering
College of Engineering
Baghdad University
Email: raedis@yahoo.com

***Abstract***—In this paper, a single-phase boost type ac-dc converter with power factor correction (PFC) technique is designed and implemented. A current mode control at a constant switching frequency is used as a control strategy for PFC converter. The PFC converter is a single-stage single-switch boost converter that uses a current shaping technique to reshape the non-sinusoidal input current drawn by the bulky capacitor in the conventional rectifier. This technique should provide an input current with almost free-harmonics, comply with the IEC61000-3-2 limits, and a system operates with near unity power factor. The other function of the boost converter that should be accomplished is to provide a regulated DC output voltage. The complete designed system is simulated in MATLAB/SIMULINK and a hardware prototype has been built using analog devices. Simulation results and experimental results are presented to validate the proposed system.

***Keywords*— Boost converter, power factor correction, power quality.**

# تصميم وتنفيذ محول رافع احادي الطور بتقنية تصحيح معامل القدرة

**أ.د. جعفر حميد علوش**
**قسم الهندسة الكهربائية**
**كلية الهندسة/جامعة بغداد**

**أ.م.د. تركي كحيوش حسن**
**قسم الهندسة الكهربائية**
**كلية الهندسة/الجامعة المستنصرية**

**م.م. رائد فؤاد عباس**
**قسم الهندسة الكهربائية**
**كلية الهندسة/جامعة بغداد**

**الخلاصة**: في هذا البحث، سيتم تصميم وتنفيذ محول رافع احادي الطور ذو تقنية تصحيح معامل القدرة. سيتم استخدام سيطرة نمط التيار بتردد ثابت كاستراتيجية للمحول. المحول المصحح لمعامل القدرة سيكون محول رافع للفولتية احادي المرحلة واحادي المفتاح والذي يستخدم تقنية تشكيل التيار ليعيد تشكيل تيار الادخال اللاجيبي المسحوب بواسطة المتسعة الكبيرة في المقوم التقليدي. يجب ان توفر هذه التقنية تيار ادخال خال من التوافقيات ويلتزم بمقاييس ال IEC61000-3-2، وتوفر كذلك نظاما يعمل بمعامل قدرة قريب من الواحد. الوظيفة الاخرى للمحول الرافع التي يجب ان تحقق هي توفير فولتية خروج منظمة. سيتم محاكاة النظام ككل باستخدام MATLAB/SIMULINK وسيتم بناء نموذج عملي له باستخدام الدوائر المتماثلة. سيتم رفد نتائج المحاكاة والنتائج العملية لتأييد النظام المقترح.

**الكلمات الرئيسية: محول رافع، تصحيح معامل القدر، جودة القدرة.**

## 1. INTRODUCTION

Power factor correction technique has been widely used in ac-dc switching-mode power supply to improve input power quality and to meet the requirement of international standards [K.-M. Ho, 2010]. Power supplies without PFC capability usually contain a diode-bridge rectifiers, which are largely used to provide dc source for the load, cause serious harmonic problem of power quality due to the nonlinearity of the diode rectifier and the capacitive filter (between the rectifier and the load). This behavior causes to draw non-sinusoidal input currents leading to inject harmonics into the utility lines and thus producing a current distortion. These effects will draw the system performance to lower power factor then reducing the maximum power available from the power lines and reducing the efficiency.

Power supplies with PFC capability usually contain a converter whose first function is to reduce the harmonics to ensure a near unity power factor at the input. For medium to high power, boost converter operated in continuous conduction mode (CCM) is the usual form of a PFC converter [G. Chu, 2009 - O. Garcia, 2003] with average current mode control (ACM). A fast control loop, known as inner current loop, is used such that the input current follows the same sinusoidal waveform as the input voltage. The PFC converter is often terminated with a storage capacitor to provide a tightly regulated output voltage to the eventual load. This is the second function of the PFC converter achieved through an outer voltage loop.

In ACM control technique [L. H. Dixon, 1990- P. C. Todd, 1999], a current error amplifier, which is a two-pole, one-zero compensation network, is used in the inner loop which increases the complexity in control system. This compensation network is difficult to analyze and synthesize and the selection of pole and zero is affected by several factors [C. Zhou, 1992]. Furthermore, a systematic derivation procedure that is applicable to both control loops (inner and outer loops) is still missing and this necessitates the use of trial-and-error procedures in the design of the control parameters [G. Chu, 2009]. The systematic derivation procedure proposed by Chu et al. [G. Chu, 2009] results in a complex control circuit due to the existing of the current reference differentiator and the use of four sensing circuit instead of three as in ACM control technique. Another category is reported in the development of the current mode technique, which is the feedforward control [S. Wall, 1997 - H.-C. Chen, 2009]. The basic idea is to generate a "nominal duty ratio pattern" to alleviate the task of the feedback controller. All the previous mentioned works used a digital controller to implement the feedforward controller.

Concerning the outer voltage loop, its design is difficult due to the presence of a relatively high ripple with twice the line frequency on the output voltage. This voltage ripple will cause a considerable distortion in the reference current generated by the voltage loop, which in turn distorted the input current. However, with a low ripple (below 10% of the output voltage), the input current distortion will be nearly disappeared when the voltage controller is designed with a low bandwidth. A poor dynamic response is the result of this approach, in other words, the output voltage will have a slow transient response with a relatively large overshoot that may add more stress on the circuit components. Many approaches have been reported in the literature to improve the transient response, but at the expense of PF, harmonic reduction, cost, complicated control circuit, or narrow load ranges. In fact, with a single stage PFC converter, it is to be nearly impracticable to achieve good dynamic response (good voltage regulator) and minimum input current distortion (good PFC) at the same time [C. K. Tse, 2005]. This is because there is a trade-off between output voltage dynamic and input current distortion. Table (1) shows the most popular techniques used to improve the transient response of the voltage loop and current harmonic reduction with their drawbacks and limitations.

In this paper, a simplified version of the feedforward controller presented in [H.-C. Chen, 2004] is used that it can be simply implemented with analog circuit. The effect of large-scale input voltage variation can be removed from the current control loop by introducing the feedforward signal and then a simple proportional (P-controller) is used in the feedback control loop. A proportional-integral (PI) controller is used in the outer loop. A simple LPF is used in the outer loop, with relatively low bandwidth, to eliminate the voltage ripples. The

complete system is designed and implement with analog circuit devices.

## 2. OPERATION PRINCIPLE OF BOOST PFC CONVERTER

Single-phase boost PFC circuit consists of a main power circuit and a control circuit as shown in Fig.1. The Power circuit mainly comprises of a full-bridge diode rectifier circuit followed by a boost dc-dc converter and a capacitor filter. A well-designed controller that controls the main switch in the converter can perform a unity power factor correction and output voltage regulation. PFC converter utilizes two-loop control structure, with an outer voltage-regulating control loop providing reference to an inner current-shaping loop. In practice, the dc link capacitance $C_o$ is large enough such that it could be treated as a voltage source. Under this assumption, dc voltage $v_o$ and the voltage loop controller output are constant.

Through the action of the inner loop controller, the inductor current is constrained to follow the rectified input voltage, resulting in a nearly sinusoidal input current waveform. As to the conventional cascade-structured feedback control system shown in Fig.2, the control signal ($v_{iL}$) is generated by regulating the voltage tracking error ($v_{err}$) through the voltage controller ($G_{cv}$) in the outer loop. By multiplying $v_{iL}$ with the rectified sine wave, $v_{rec}$, a current reference $i_{ref}$ is yielded. Then, the switching control of inductor current is obtained by comparing the current controller ($G_{ci}$) output, which is denoted by ($v_{cont}$), with a fixed frequency triangular wave ($v_{tri}$) through a PWM (pulse width modulator) comparator to achieve the line current shaping.

## 3. DESIGN SPECIFICATIONS

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency must be specified. To simplify the analysis of the converter for high PF operation with low line current total harmonic distortion, the following assumptions are made:

- The power switch and the diode are ideal switches and the switching losses are neglected.
- Parasitic components of the inductor and the output capacitor are neglected.

The design of the boost PFC converter is made on the basis of the following specifications:

- Input voltage range (rms): 85-135 V
- Line frequency ($f_{line}$): 50 Hz
- Output voltage ($V_o$): 325 V
- Maximum output power ($P_{o\_max}$): 750 W
- Switching frequency ($f_s$): 30 kHz

## 4. POWER STAGE DESIGN

**4.1. Boost Inductor:** The required inductor value of the boost converter is determined by the amount of switching ripple current that can be tolerated. Allowing more ripples will reduce the inductor value, but this will increase input line noise and the peak current through the diode rectifier, and switch. The peak-to-peak ripple current in the inductor is chosen to be 15% of the maximum peak line current. For lossless converter, the maximum peak current occurs at the peak of the minimum line voltage is given by: **[**P. C. Todd, 1999**]**

$$I_{s\_max} = \frac{\sqrt{2}P_{o\_max}}{V_{rms\_min}} = \frac{\sqrt{2} \times 750}{85} = 12.47 \text{ A} \quad (1)$$

The peak-peak ripple current can be determined as:

$$\Delta i_L = 12.47 \times 0.15 = 1.87 \text{ A} \quad (2)$$

The duty cycle at the peak input voltage is calculated by using **[**L. H. Dixon, 1990**]**:

$$d = \frac{V_o - V_{rec}}{V_o} = \frac{325 - \left(\sqrt{2} \times 85\right)}{325} = 0.63 \quad (3)$$

where $V_{rec}$ denotes the peak of the rectified voltage

Then, the inductor value can be evaluated as **[**P. C. Todd, 1999**]**:

$$L = \frac{V_{rec}\, d}{\Delta i_L f_s} = \frac{\left(\sqrt{2} \times 85\right)(0.63)}{(1.87)(30 \times 10^3)} = 1.35 \text{ mH} \quad (4)$$

In order to have a safety margin, the value of *L* was chosen to be 1.5 mH.

**4.2. Output Capacitor:** There are many factors that influence the value of the output capacitor. The output voltage hold-up time, the output ripple voltage, the outer-loop transient response and the input current harmonic distortion are all dependent to some degree on the value of the output capacitor **[**P. C. Todd, 1999**]**. A larger value of the output

capacitance results in better performance but this can increase the cost and size. Another constraint, the inrush current, should be taken into consideration when one intends to increase the output capacitor in PFC applications. At starting, with a large capacitor value, the inrush current increases in peak magnitude and period. However, hold-up time and voltage ripple, are the major factors affecting capacitor selection. The minimum value of the output capacitor can be determined by choosing the minimum value of the output voltage ($V_{omin}$) and the minimum value of the hold-up time ($t_h$). Accordingly, $V_{o\_min}$ is considered to be 260 Volt. In respect of $t_h$, it is considered here to be 45msec that means if the nominal output voltage $V_o$ is 325 Volt, then, during the input supply turns-off, the capacitor voltage will drop to 260 Volt within 45msec. Now, $C_o$ can be calculated as **[**P. C. Todd, 1999**]**:

$$C_o = \frac{2P_o t_h}{V_o^2 - V_{o\_min}^2} = \frac{2(750)(45 \times 10^{-3})}{325^2 - 260^2} = 1775\ \mu F \quad (5)$$

The above calculated value of $C_o$ may be approximated to the standard value 2000μF.

## 5. INNER CURRENT CONTROL LOOP

**5.1. Controller Design:** In the current control scheme shown in Fig. 3, the feedback controller ($G_{ib}$) is augmented with a command feedforward controller ($G_{iff}$) which is used to reduce the command tracking error. Considering that the converter is operated in CCM and the output voltage is ripple-free due to the sufficiently large capacitor $C_o$, and well regulated such that it is assumed to be equal to the voltage reference $V_{ref}$, the differential eq. (6), which represents the state space average model of the power stage that derived in **[**R. F. Abbas, 2012**]**, is expressed as:

$$L\frac{di_L}{dt} = v_{rec} - (1-d)V_{ref} \quad (6)$$

According to Fig.3, the duty ratio $d$ can be expressed as

$$d = \frac{v_{cont}}{V_{tri}} = \frac{v_{contb} + v_{contff}}{V_{tri}} \quad (7)$$

where $V_{tri}$ denotes the amplitude of the sawtooth signal, $1/V_{tri}$ is the gain of PWM unit. The command feedforward control ($v_{contff}$) can be given as: **[**R. F. Abbas, 2012**]**

$$v_{contff} = V_{tri}\left(1 - \frac{v_{rec}}{V_{ref}}\right) \quad (8)$$

By substituting (7) and (8) into (6), the current equation will be simply given as:

$$\frac{di_L}{dt} = \frac{V_{ref}}{LV_{tri}} v_{contb} \quad (9)$$

Due to the linear nature, eq. (9) can be expressed in the s-domain as:

$$i_L(s) = \frac{V_{ref}}{sLV_{tri}}\ v_{contb} \quad (10)$$

Eq. (10) defines the current loop dynamic model shown in Fig.4 at nominal case after introducing the command feedforward control. The effect of input voltage variation in the average model of the power stage had been removed by introducing the feedforward signal $v_{contff}$ in the control loop. Furthermore, the equivalent plant model in the Fig.4 is a first-order model. It means that a simple proportion-type (P-controller) can be used in the current controller, that is, $G_{ib}(s) = k_{pi}$ where $k_{pi}$ denotes the proportional gain.

**5.2. Frequency Response Analysis:** From Fig.4, the open loop $G_{iOL}(s)$ and closed loop $G_{iCL}(s)$ transfer functions can be expressed as:

$$G_{iOL}(s) = \frac{k_{iL}k_{pi}V_{ref}}{LV_{tri}s} \quad (11)$$

$$G_{iCL}(s) = \frac{i_L(s)}{i_{ref}(s)} = \frac{k_{pi}V_{ref}}{LV_{tri}s + k_{iL}k_{pi}V_{ref}} \quad (12)$$

where $k_{iL}$ denote the sensing gain of the inductor current.

To achieve tight control, and good dynamic performance of the inductor current, the current loop must have high low-frequencies gain and wide bandwidth. For the utility line frequency ($f_{line}$=50Hz), the gain crossover frequency ($f_{ci}$) should be $\gg 2f_{line}$ **[**H.-C. Chen, 2004**]** and may not be larger than 1/5 of the switching frequency $f_s$ **[**K. P. Louganski, 2007**]**. If the current loop is designed with low $f_{ci}$ (close to $2f_{line}$), a zero-crossing distortion of the line current waveform appears due to the leading phase of the current relative to the line voltage. This leading phase is a result of control action of the current loop compensation scheme **[**J. Sun, 2004**]**. The current loop dynamic response should be designed depending on the crossover frequency $f_{ci}$.

From eq. (11), the unity gain crossover frequency can be found as:

$$f_{ci} = \frac{k_{iL} k_{pi} V_{ref}}{2\pi L V_{tri}} \quad (13)$$

By determining the crossover frequency, the parameter of P-controller ($k_{pi}$) can be found from eq. (13). The crossover frequency is chosen here to be 1/6 of the switching frequency $f_s$, that is $f_{ci} = 5kHz$. Values of $V_{tri}$ and $k_{iL}$ are chosen to be 3.2 and 0.1 respectively, then $k_{pi}$ can be calculated as:

$$k_{pi} = \frac{\pi L\, f_s V_{tri}}{3 k_{iL} V_{ref}} \quad (14)$$

According to (14), $k_{pi}$ is calculated to be 4.6.

## 6. OUTER VOLTAGE CONTROL LOOP

**6.1. Controller Design:** A simple proportional-plus-integral (PI) type controller is used to control the outer voltage loop. the dc side capacitor voltage ($v_o$) is fed back and compared with a control reference, and the error $v_{err}$ is compensated by the PI-controller to produce $v_{iL}$ which in turn provides the reference current to the inner-loop through multiplying it by a rectified sine wave signal $s(t)$ as shown in Fig.5. The PI controller acts upon the error $v_{err}$ with parallel proportional and integral responses in an attempt to drive the error to zero. The transfer function of the PI-controller can be expressed as:

$$G_{cv}(s) = k_p + \frac{k_i}{s} = k_p \frac{s + \omega_z}{s} \quad (15)$$

where $k_p$ and $k_i$ are the proportional and integral gains, respectively, $\omega_z$ is the angular frequency of the zero in the PI controller and $\omega_z = k_i/k_p$.

To design the outer loop controller, it is assumed that the inner loop is unity; the inductor current $i_L$ has tracked the reference current $i_{ref}$, as illustrated in Fig.5. Then, referring to Fig.6, the open loop transfer function of the outer loop $G_{vOL}(s)$ can be expressed as:

$$G_{vOL}(s) = G_{cv}(s) G_{pv}(s) k_{vo} \quad (16)$$

The small signal control-to-output voltage transfer function ($G_{pv}(s)$), which can be used to design the voltage loop, has been derived in [R. F. Abbas, 2012] as:

$$G_{pv}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{iL}(s)} = \frac{k_{vi} k_f^2}{k_{Vff}^2 k_{iL} V_o} \frac{R}{2 + RC_o s} \quad (17)$$

Now, substituting (15) and (17) into (16) yields:

$$G_{vOL}(s) = \frac{k_{vi} k_f^2 k_{vo}}{k_{Vff}^2 k_{iL} V_o} \frac{R k_p (s + \omega_z)}{RC_o s^2 + 2s} \quad (18)$$

where $k_{vi}$, $k_{vo}$, $k_{Vff}$ denote the scaling factors of the rectified input voltage, output voltage, and the input voltage feedforward respectively. $k_f$ denotes the form factor (rms / average) of the full wave rectified voltage which equal to 1.11 ($\pi/2\sqrt{2}$) and expressed as:

$$k_f = \frac{V_{rms}}{V_{ff}} \quad (19)$$

where $V_{rms}$ is the rms of the input supply, $V_{ff}$ denotes the output signal of the input voltage feedforward circuit which represents the average of the rectified input voltage. This feedforward voltage is essential to remove the effect of input voltage variation by generating a rectified sine wave signal $s(t)$ [M. H. Rashid, 2007].

**6.2. Frequency Response Analysis:** To determine the PI Parameters $k_p$ and $k_i$, the outer-loop is compensated to satisfy the following design requirements:

- Unity gain crossover frequency ($f_c$) is greater than 5Hz.
- Phase margin ($\phi_m$) > 45°.
- Overshoot is less than 20%.
- Settling time is below 125msec.

By using the circuit parameters in table (2), the open loop $G_{vOL}(s)$ and the closed loop $G_{vCL}(s)$ transfer function can be given as:

$$G_{vOL}(s) = 0.0258 \frac{R k_p (s + \omega_z)}{0.002 R s^2 + 2s} \quad (20)$$

$$G_{vCL}(s) = \frac{\left(G_{vOL}(s)\right)_{\text{unity feedback}}}{1 + k_{vo}\left(G_{vOL}(s)\right)_{\text{unity feedback}}} = \frac{1.679 R k_p s + 1.679 R k_p \omega_z}{0.002 R s^2 + \left(2 + 0.0258 R k_p\right) s + 0.0258 R k_p \omega_z} \quad (21)$$

Using Eqs. (20) and (21), Bode plots of the voltage loop can be computed in matlab program. The frequency and step response of the outer loop

will be examined, at full-load (750W), according to the unity gain crossover frequency ($f_c$) and phase margin $\phi_m$. First, the value of $\phi_m$ is to be maintained on $60^\circ$, and $f_c$ is to be changed in the range of (3-25Hz) as in Fig.7. The figure shows that the increasing in $f_c$ improves the dynamic response (by decreasing the settling time ($t_s$)) but on the other hand, the peak response (maximum overshoot ($M_p$)) is increased. This requires a compromise between the peak response and settling time. Initially, the crossover frequency will be chosen to be $f_c = 10Hz$, which gives $M_p = 21.4\%$ and $t_s = 138ms$.

Then, as shown in Fig.8, the value of $f_c$ is now maintained on 10Hz, and $\phi_m$ is to be changed in the range of $(30^\circ - 80^\circ)$. The peak response is indirectly proportional to the variation in $\phi_m$ but the proportionality between $\phi_m$ and $t_s$ is irregular. The minimum value of settling time ($t_s = 121ms$) is obtained with $\phi_m = 70°$ for allowable tolerance within 2%. Concerning the maximum overshoot $M_p$, it is found to be 15% for $\phi_m = 70°$ which is acceptable according to the design requirements. Then with $f_c = 10Hz$ and $\phi_m = 70°$, PI parameters is computed as $k_p = 4.3$ and $\omega_z = 31$ ($k_i = 136$).

The loop dynamic response is then examined for different load conditions. The open loop response in Fig.9 shows that at full-load and at $f_c = 10$Hz, the phase angle ($\phi_p$) equals $-110^\circ$ (or $\phi_m = 70^\circ$). As the load decreases, the phase margin is slightly decreased and at 200W it reaches $65^\circ$ ($\phi_p = -115$). For the step response, Fig.9, the maximum overshoot $M_p$ fluctuates between 14.6% at full-load and 19.9% at 200W. The settling time is slightly varying between 120ms and 118ms.

The outer-loop bandwidth (located at $-3dB$ below the DC-gain) can be determined from the closed loop frequency response shown in Fig. 10. The bandwidth of the outer-loop is slightly varying between $12.5Hz$ at full-load and $13.1Hz$ at 200W output power.

## 7. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the designed system, a simulation performed by MATLAB/SIMULINK has been used and a hardware prototype has been built and tested. The simulation and experimental results are obtained and discussed in this section. The parameters and component values of the designed system are summarized in Table 2. A laboratory prototype of the boost PFC converter and the control circuit are constructed using analogue devices (see the appendix) with schematic circuit diagram shown in Fig.11.

For simulation, Fig.12 shows the line current and the line voltage. Under full-load (750W), it was found that, in the steady state, a near sinusoidal input current was obtained with the total harmonic distortion of the input current ($THD_i$) equals to 2.9% and the input power factor (PF) is 0.999. For 200W load, $THD_i$ and PF are found to be 10.8% and 0.991 respectively. Fig.13 shows the harmonic spectrum of the line current at full-load. Under the load change, Fig.14 shows the output voltage and the input current response when the load changes from 300W to 750W and in contrary. The overshoot of the output voltage is within 4% (13V above and below the steady state value) and settles within 100ms.

For experimental results, Fig.15 shows the input line current and the input line voltage waveforms. Under full-load (750W), it was found that, in the steady state, a near sinusoidal input current was obtained with the total harmonic distortion of the input current ($THD_i$) equals to 3% and the input power factor (PF) is 0.996. For 200W load, $THD_i$ and PF are found to be 14.1% and 0.98 respectively. Fig.16 shows the harmonic spectrum of the input line current at full-load. Under the load step change, Fig.17 shows the output voltage and the inductor current responses when the load changes from 350W to 750W and in contrary. The overshoot of the output voltage is found within 6.5% (21V above and below the steady state value) and settles within 100ms and 125ms for changing from 300W to 750W and from 750W to 300W respectively.

The measured harmonic components of the line input current given in Fig.17 is compared with the IEC 61000-3-2 Class A standard **[**IEC 61000, 1998**]**. Fig.18 shows that the measured harmonic components (rms) of the input current ($I_{n\_rms}$), expressed as a percent of the rms fundamental current ($I_{1\_rms}$), are much lower than those of the IEC limits. Fig.19 shows the boost PFC converter performance in terms of PF, $THD_i$, and converter efficiency when the output power $P_o$ varies from 200W to full-load (750W). The recorded input PF is found to be near unity and the THD of input current is

complied with IEC 61000-3-2 regulation. In spite of the hard switching operation, the single phase boost PFC shows good performance in terms of efficiency.

The system is tested with 85V and 135V input voltage at full-load operation. THDi and PF are found to be 5.4% and 0.988 respectively for 85V input voltage. For 135V, THDi and PF are found to be 3.2% and 0.991 respectively.

## 8. CONCLUSION

In this paper, a single stage single switch PFC converter has been designed to improve the power quality to be complied with the IEC 61000-3-2 Class A limits. The power factor has been recorded to be within 0.996-0.98 and the $THD_i$ is found to be 3%-14.1%. A current mode control at a constant switching frequency has been used as a control strategy for PFC converter. In the current control scheme, the feedback controller is augmented with a command feedforward controller which simplifies the current controller design. The controller parameters have been designed depending on the frequency response analysis. A hardware prototype has been built to verify the designed system. The experimental results showed good agreement with the analytical and simulated results.

## REFERENCES

A. Fernandez, J. Sebastian, M. M. Hernando, P. Villegas, and J. Garcia, "Helpful hints to select a power-factor-correction solution for low- and medium- power single-phase power supplies," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 46–55, Feb. 2005.

A. Fernandez, J. Sebastian, and P. Villegas, "Dynamic limits of a power-factor preregulator," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 77–86, Feb. 2005.

A. Prodic´, "Compensator Design and Stability Assessment for Fast Voltage Loops of Power Factor Correction Rectifiers," IEEE Trans. Power Electron. vol. 22, no. 5, pp. 1719–1730, Sep. 2007.

C. K. Tse, "Circuit Theory and Design of Power Factor Correction Power Supplies," IEEE Distinguished Lecture 2005, Circuits and Systems.

C. Zhou and M. M. Jovanovic, "Design trade-offs in continuous current mode controlled boost power factor correction circuits," in Proc. High Freq. Power Conv. Conf. HFPC'92, May 1992, pp. 209–220.

Electromagnetic Compatibility (EMC)–Part 3: Limits-Section2: Limits for Harmonic Current Emissions (Equipment Input Current <16 A per-Phase), IEC 61000-3-2, 1998.

G. Chu, C. K. Tse, S. C. Wong, and S.-C. Tan, "A Unified Approach for the Derivation of Robust Control for Boost PFC Converters," IEEE Trans. Power Electron., vol. 24, no. 11, pp. 2531–2544, Nov. 2009.

G. Spiazzi, P. Mattavelli, and L. Rossetto, "Power factor Preregulators with improved dynamic response," IEEE Trans. Power Electron., vol. 12, no. 2, pp. 343–349, Mar. 1997.

H.-C. Chen, H.-Yi Li, and R.-S. Yang, "Phase Feedforward Control for Single-Phase Boost-Type SMR," IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1428-1432, May. 2009.

H.-C. Chen, S. H. Li, and C. M. Liaw, "Switch-mode rectifier with digital robust ripple compensation and current waveform controls," IEEE Trans. Power Electron., vol. 19, no. 2, pp. 560-566, Mar. 2004.

J. Sebastian, D. G. Lamar, M. M. Hernando, A. R.-Alonso, and A. Fernandez, "Steady-State Analysis and Modeling of Power Factor Correctors with Appreciable Voltage Ripple in the Output-Voltage Feedback Loop to Achieve Fast Transient Response," IEEE Trans. Power Electron. vol. 24, no. 11, pp. 2555–2566, Nov. 2009.

J. Sun, "On the zero-crossing distortion in single-phase PFC converter," IEEE Trans. Power Electron., vol. 19, no. 3, pp. 685–692, May 2004.

K.-M. Ho, C.-A. Yeh, and Y.-S. Lai, "Novel Digital-Controlled Transition Current-Mode Control and Duty Compensation Techniques for Interleaved Power Factor Corrector," IEEE Trans. Power Electron. vol. 25, no. 12, pp. 3085–3094, Dec. 2010.

K. P. Louganski and J. S. Lai, "Current phase lead compensation in single-phase PFC boost converters with a reduced switching frequency to line

frequency ratio," IEEE Trans. Power Electron., vol. 22, no. 1, pp. 113–119, Jan. 2007.

L. H. Dixon, "Average current mode control of switching power supplies," Unitrode, Watertown, MA, Appl. Note U-140, 1990.

L. H. Dixon, "High power factor switching pre-regulator design optimization," Texas Instruments, Dallas, Unitrode Power Supply Des. Semin. Manual SEM700, 1990.

M. H. Rashid, "Power Electronics Handbook," 2nd ed., Academic Press, San-Diego, 2007.

O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 749–755, May 2003.

P. C. Todd, "UC3854 Controlled, Power Factor Correction Circuit Design," Unitrode Corp., Merrimack, NH, Appl. Note U-134, pp. 3-269–3-288, 1999.

P. C. Todd, "Boost Power Factor Corrector Design with the UC3854," Unitrode Corp., Merrimack, NH, Appl. Note U-159, 1999.

R. F. Abbas, "Single-Phase Boost Power Factor Corrected Converter for Induction Motor Drive," M.Sc. Thesis, Baghdad University, Baghdad, 2012.

R. Ghosh and G. Narayanan, "Generalized feedforward control of single-phase PWM rectifiers using disturbance observers," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 984–993, Apr. 2007.

S. Wall and R. Jackson, "Fast controller design for single-phase power-factor-correction systems," IEEE Trans. Ind. Electron., vol. 44, no. 5, pp. 654–660, Oct. 1997.

Table (1) Different techniques for voltage loop dynamic improvement

| Technique | description | Drawback and limitation |
|---|---|---|
| Conventional two-stage converters | Second stage is connected in cascade with the PFC converter to provide fast response. | High cost, large size, low efficiency, and complicated control circuit particularly in low-power applications [ A. Fernandez, 2005] |
| Voltage ripple filtering | LPF: notch, or comb filter inserted before or after the voltage controller | Cannot eliminate the 4th and higher order harmonics in the output voltage. For notch, or comb filter, to eliminate the 4th harmonics, analog implementation is difficult due to its complex structure and digital implementation requires large memory storage.[ R. Ghosh, **2007]** Give a trade-off between improving the dynamic response and current distortion [ A. Fernandez, 2005] |
| Voltage ripple cancellation | The ripple is eliminated by modifying the voltage reference with a component having the same amplitude and opposite sign of the sensed voltage ripple. | Not easily implemented in low-cost PFCs. [ J. Sebastian, 2009] Give a trade-off between improving the dynamic response and current distortion. [ G. Spiazzi, 1997] Current distortion increased during disturbance, so that, additional circuit is required which complicate the control circuit |
| Regulation band and dead-zone controllers | Depending on the amplitude of the voltage-loop error signal, bandwidth of voltage loop is kept low at steady state to obtain a sinusoidal input current. During transients, it is increased to have a good dynamic response. | For small errors, approximately equal to the ripple magnitude, the loop is either slow or completely insensitive to voltage variations and hence the system suffers from regulation problem [A. Prodic´, 2007]. Have limit cycle oscillations at light loads [R. Ghosh, **2007]** |

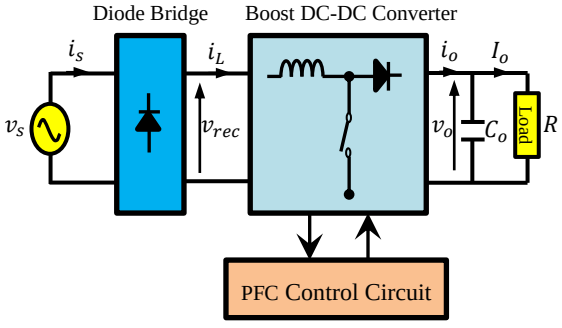



Fig.1 Block diagram of boost PFC converter

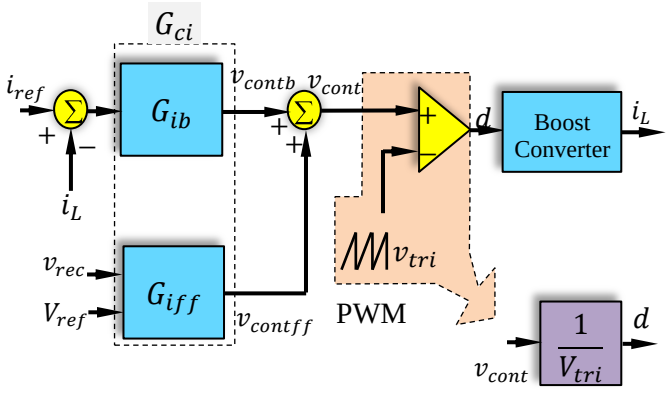



Fig.3 Current control scheme

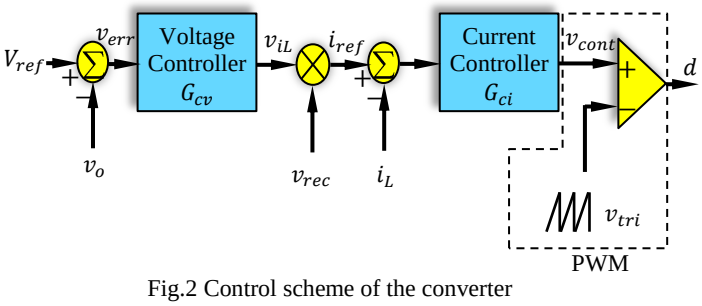



Fig.2 Control scheme of the converter

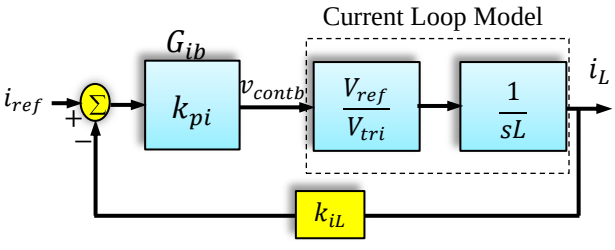



Fig.4 Equivalent current-loop control

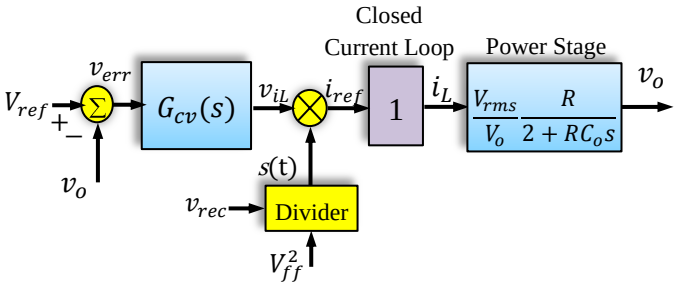



Fig.5 Voltage control scheme

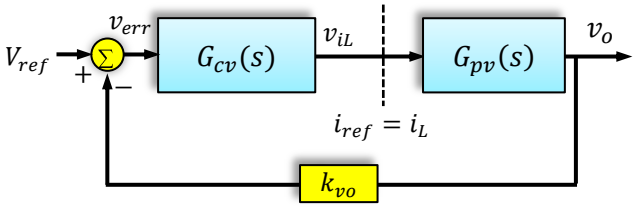



Fig.6 Block diagram of the voltage loop

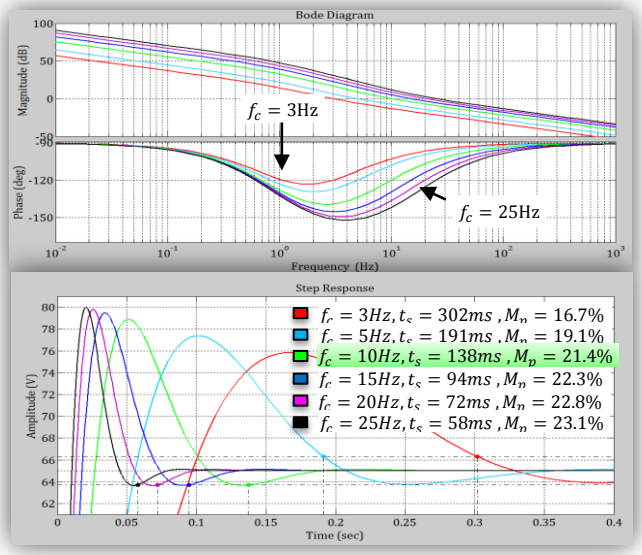



Fig.7 Outer loop frequency response at full-load, $\phi_m = 60°$ for different values of $f_c$ ; upper: open loop, lower: step response

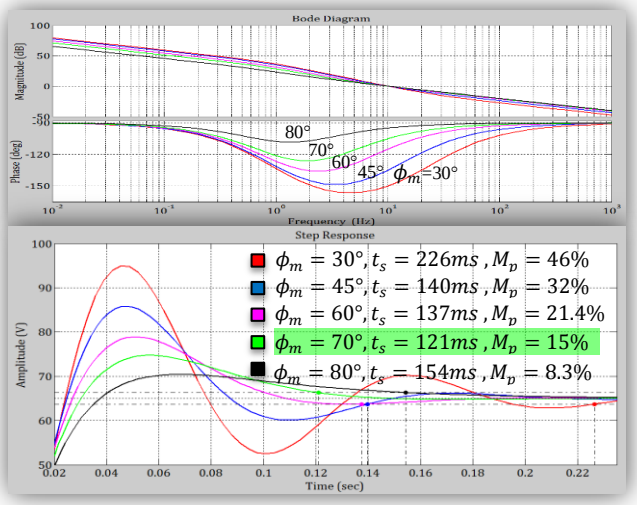



Fig.8 Outer loop frequency response at full-load, $f_c$=10Hz for different values of $\phi_m$ ; upper: open loop, lower: step response

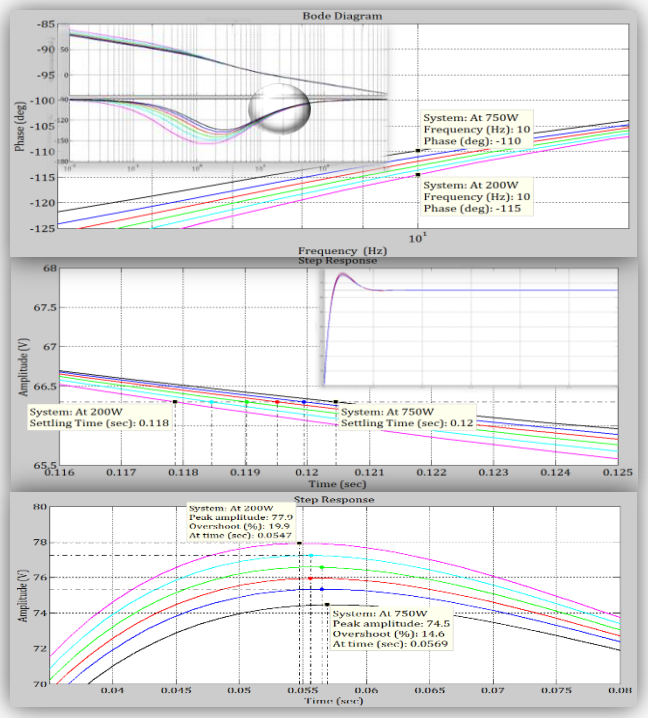



Fig.9 Frequency response of the outer loop, with $k_p$ = 4.3 and $k_i$ = 136 for different load conditions; upper: open loop, middle: step response shows $t_s$, lower: step response shows $M_p$

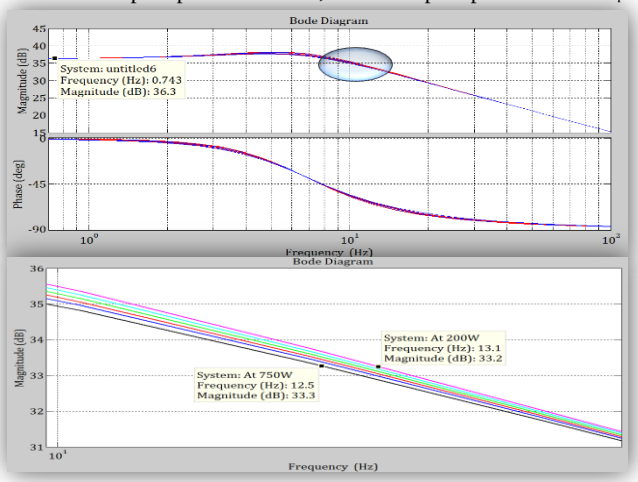



Fig.10 Outer loop frequency response with $k_p$ = 4.3 and $k_i$ = 136 for different load conditions; upper: closed loop, lower: a magnified section of the magnitude in (upper) shows the loop bandwidth

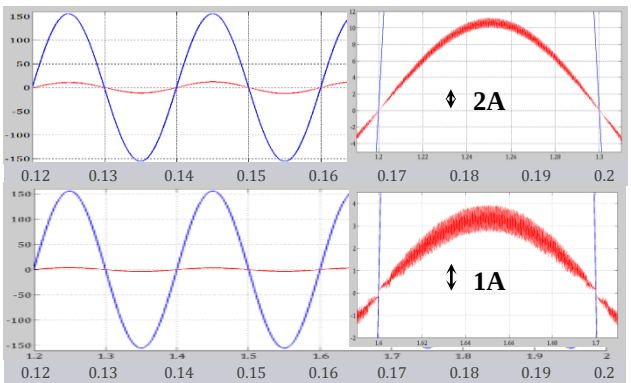



Fig.12 Steady state of input current and input voltage waveforms; upper: at 750W, lower: at 200W

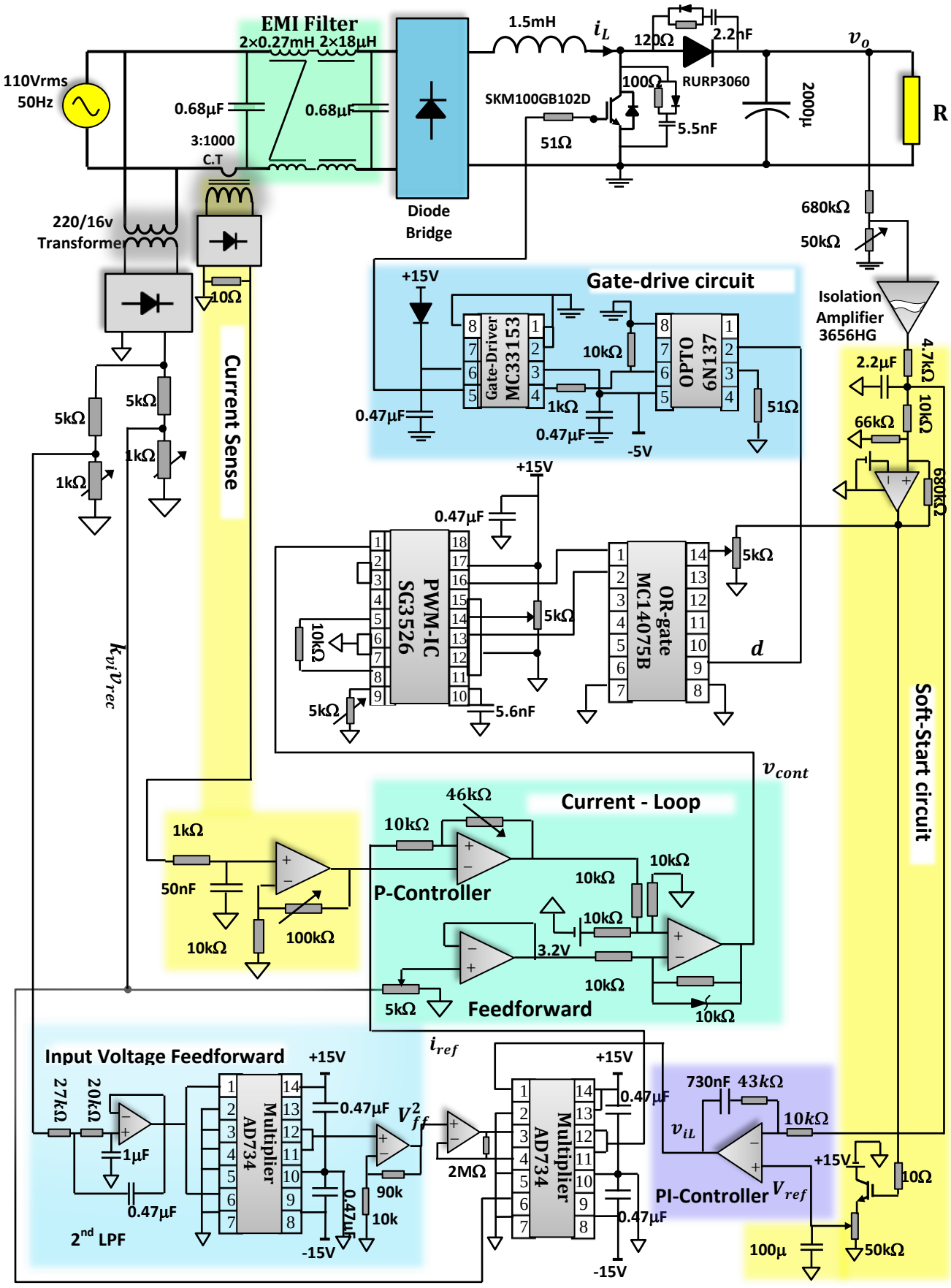



Fig.11 Full schematic diagram of the boost PFC converter circuit

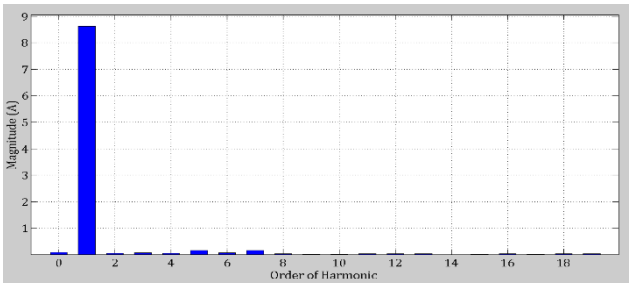



Fig.13 Harmonic spectrum of the line current (rms) at full-load

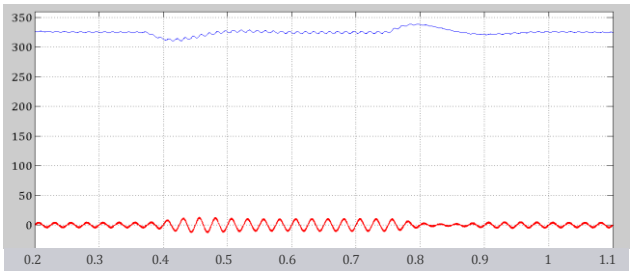


Fig.14 Waveforms of output voltage $v_o$ and input current $i_s$ when the load steps from 300W to 750W (upper: $v_o$ 50V/div; lower: $i_s$ 50 A/div).

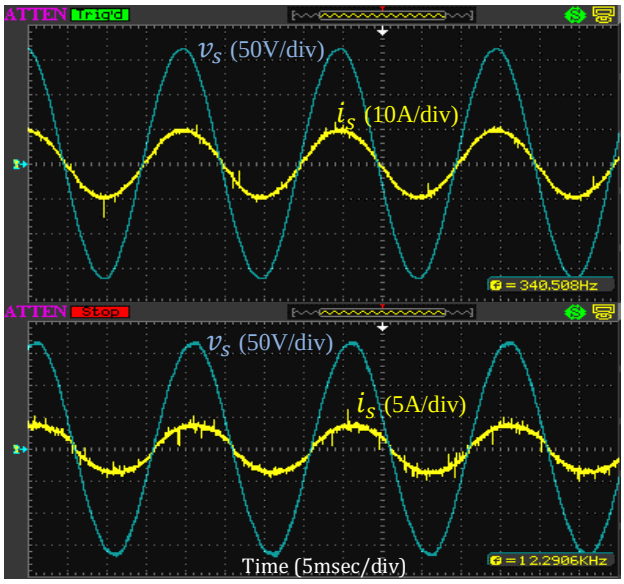



Fig.15 Steady state of the measured input current and input voltage waveforms; upper: at 750W, lower: at 200W

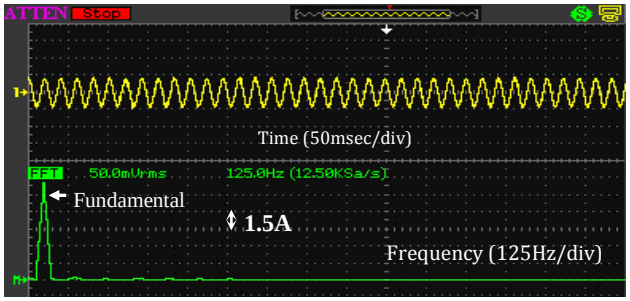



Fig.16 Harmonic spectrum of the measured input line current (rms) at full-load

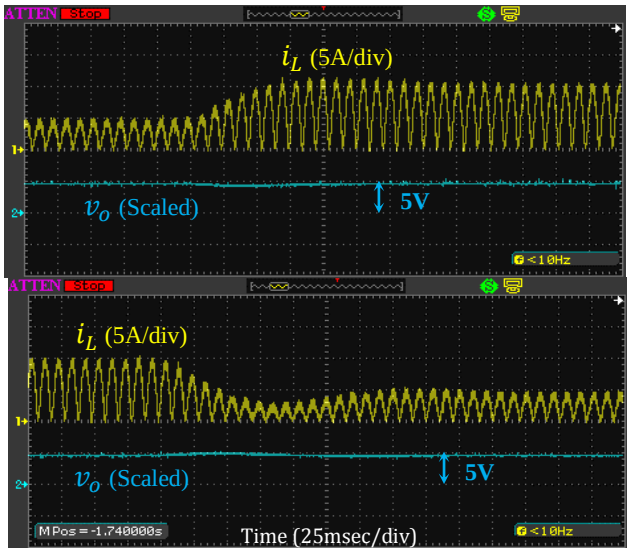



Fig.17 Waveforms of output voltage $v_o$ and inductor current $i_L$ under the load change; upper: from 350W to 750W, lower: from 750W to 350W

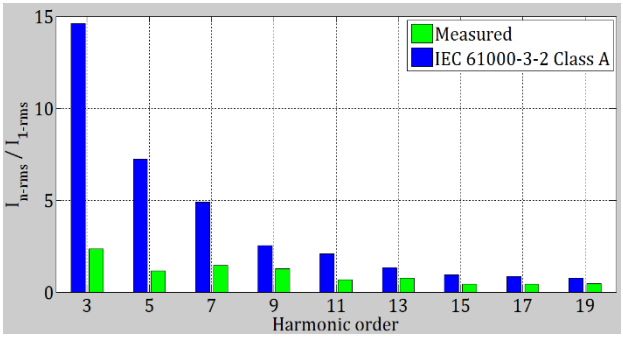



Fig.18 Measured harmonic content of the input current at full-load versus IEC 61000-3-2 Class A limits

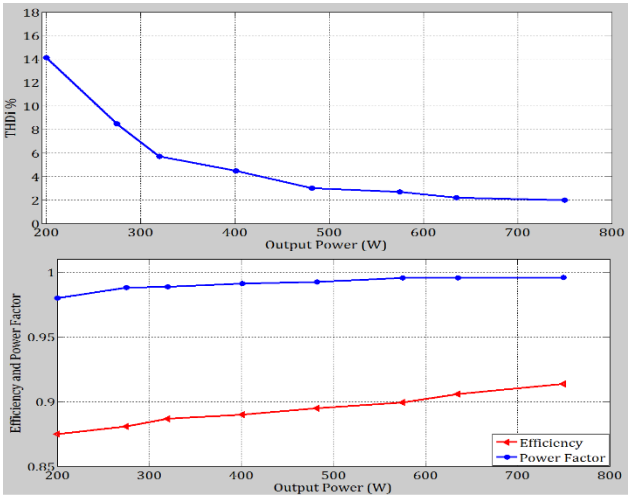
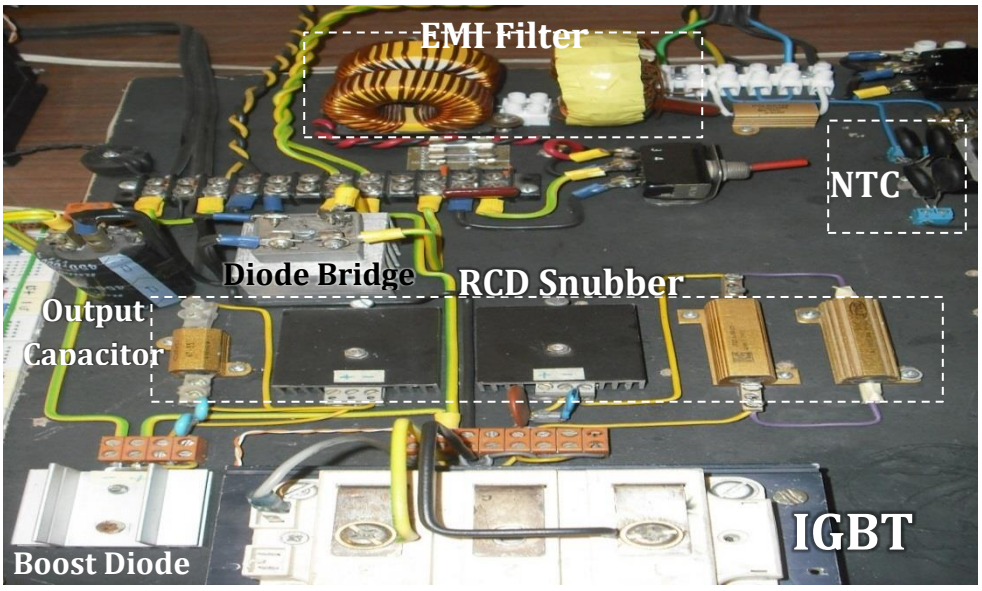



Fig.19 PFC converter performance with respect to the output power; upper: $THD_i$ vs. $P_o$, lower: efficiency and PF vs. $P_o$

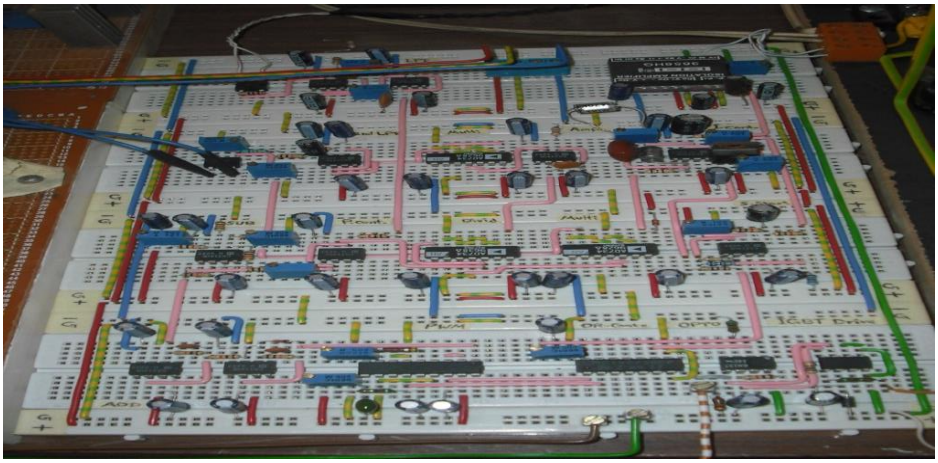
Table 2 Specifications of the designed system

| parameter | value | unit |
|---|---|---|
| Nominal line voltage ($V_{rms}$) | 110 | V |
| Converter output voltage ($V_o$) | 325 | V |
| Line frequency ($f_{line}$) | 50 | Hz |
| Switching frequency ($f_s$) | 30 | kHz |
| $k_{pi}$ | 4.6 | — |
| $k_p$ | 4.3 | — |
| $k_i$ | 136 | — |
| Maximum output power ($P_o$) | 750 | W |
| Boost inductor ($L$) | 1.5 | mH |
| Output capacitor ($C_o$) | 2000<br>450 | μF<br>V |
| Current sensing gain ($k_{iL}$) | 0.1 | — |
| Input voltage gain ($k_{vi}$) | 0.02258 | — |
| Feedforward gain ($k_{vff}$) | 0.02258 | — |
| Output voltage gain ($k_{vo}$) | 0.01666 | — |

## APPENDIX: Setup Photos




(a)



(b)

System setup (a) Power circuit (b) control circuit