COMPARATIVE STUDY OF TRADITIONAL PWM INVERTERS AND MULTILEVELS INVERTERS

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ABSTRACT:

The need of higher powers in electrical drives has forced the researchers to develop new power source possibilities. Multilevel inverters have been presented as a cost effective solution for various high voltage and high power applications including power quality and motor drive problems.

The traditional pulse width modulated (PWM) Inverter does not completely eliminate the unwanted harmonics in the output waveform. Using the multilevel inverter as an alternative to traditional PWM inverters for electric motor drive applications is investigated.

The concept of the Optimized Harmonic Elimination Stepped-Waveform (OHESW) technique for a multilevel inverter is presented. The effectiveness of this technique in minimizing the inverter switching losses and its output voltage harmonic content which cause reducing harmonic losses and torque pulsations of an induction motor fed form is investigated analytically.

Comparison between the Selective Harmonic Eliminated PWM (SHEPWM) as a traditional PWM technique for three-level inverter and the OHESW technique for multilevel inverter with regard to the switching losses, harmonic distortion, additional harmonic losses in the motor and the pulsating torques is also presented.

الخلاصة :

أن الحاجة للقدرات العالية في المسوقات الكهربائية أجبرَت الباحثين لتطوير أمكانيات جديدة لمصدر القدرة. تمّ أبداء العواكس المتعددة المستويات كحلّ فعّال ومناسب لمختلف تطبيقات القدرة العالية والفولتية العالية ومنها مسائل سوق المحرك وجودة القدرة.

التضمين التقليدى لعرض النبضة لا يحدف التوافقيات الغير مرغوب بها من الموجة الخارجة بشكل تام. تمّ تحقيق أستخدام العاكس متعدد المستويات كبديل عن العواكس التقليدية التي تعمل بتضمين عرض النبضة في تطبيقات سوق المحرك الكهربائي.

تمّ أبداء مفهوم تقنية الموجة المثالية الخطوية لحدف التوافقيات (OHESW) لعاكس متعدد المستويات. تمّ التحقق تحليلياً من فعالية هده التقنية في تقليل خسائر التشغيل في العاكس والمحتوى التوافقي للفولتية الخارجة منه والدي يؤدي الي تقليل الخسائر التوافقية والعزوم التنبضية لمحرك حثي يغدى من دلك العاكس.

تمّ أبداء مقارنة بين تضمين عرض النبضة بحدف التوافقيات الأنتقائي (SHEPWM) كتقنية تضمين تقليدية لعاكس ثلاثي المستويات وتقنية الموجة المثالية الخطوية لحدف التوافقيات لعاكس متعدد المستويات, من حيث خسائر التشغيل والتشويه التوافقي الكلي والخسائر التوافقية الأضافية والعزوم التنبضية في المحرك.

KEYWORDS

Harmonic Elimination, PWM, Multilevel Inverter.

INTRODUCTION:

In the industry, there are two basic needs for the development of the power electronic devices. The needs are a higher power capability (over 1 MW) and a smoother output voltage. In a classical 2- or 3-level low power inverter increasing the switching frequency and modifying the modulation techniques have been executed for a smoother output voltage. In the case of the high power applications, the switching frequency cannot be increased, because of higher switching losses and electronic limitation of the power switches (turn on and off times are bigger with high voltage switches than with low voltage switches). One solution for this problem is a multilevel inverter. In the multilevel inverters the voltage rating of power switches can be lower than in 2- or 3-level inverters. Lower voltage rating of switches, decrease the switching losses and diminish the electronic limitation of the high voltage switches. Increasing the voltage levels of an inverter can solve the problems of a 2- or 3-level inverter [*M. Jokinen* 2005].

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The poor quality of current and voltage fed by a classical 2- or 3-levels inverter which has been pointed out in previous works [*P. N. Enjeti* 1990, *H. S. Patel* 1973, and *J. Sun* 1992] leads to the use of multilevel inverters in the drives community, for high power adjustable speed systems.

Traditional PWM inverters have recently been found to be a major cause of motor bearing failures due to excessive bearing currents in inverter-motor drive systems [*J. M. Erdman* 1996].
One of the problems of the PWM controlled AC motors is the acoustic noise that could become unacceptable when used in silent environments [*S. Laurentiu* 2002]. Traditional PWM schemes have the inherent problems of producing Electromagnetic Interference (EMI). Rapid changes in voltages (dv/dt) are a source of EMI. The presence of a high dv can cause damage to electrical motors [*J. M. Erdman* 1996].

The Selective Harmonic Eliminated PWM (SHEPWM) technique is currently applied in conventional 2- or 3-level inverter circuits. The concept of the SHEPWM technique will be presented in this paper.

Multilevel inverters synthesize the AC voltage from several different levels of DC voltages. Each additional DC voltage level adds a step to the AC voltage waveform. Therefore, a staircase (stepped) waveform can be produced which approaches the sinusoidal waveform with minimum Total Harmonic Distortion (THD) [*J. S. Lai* 1996]. A harmonic distortion decreases when the number of voltage levels increase. This means that there is no need for such filters, which are implemented nowadays. With the multilevel inverter, also, dv/dt decrease. Smaller dv/dt decreases the motor failures like bearing failures and insulation breakdowns [*M. Jokinen* 2005].

The Optimized Harmonic Elimination Stepped-Waveform (OHESW) technique is very suitable for a multilevel inverter circuit. By employing this technique along with the multilevel topology, the low THD output waveform without any filter circuit is possible. Switching devices, in addition, turn on and off only one time per cycle, this can overcome the switching loss problem, as well as EMI problem [*S. Sirisukparsert* 1999].

The objective of this paper is to compare the results of the multilevel inverter using cascaded-inverters with OHESW technique to those of the traditional 3-level full-bridge inverter with SHEPWM technique to get the optimum one.

MULTILEVEL INVERTER ADVANTAGES AND DISADVANTAGES:

The most attractive features of multilevel inverters are as follows:

* They can generate output voltages with extremely low distortion and lower *dv*/*dt*.
* They draw input current with very low distortion.
* They generate smaller Common Mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
* They can operate with a lower switching frequency [*J. Rodriguez* 2002].

Compared to a full bridge inverter which can generate 2- or 3- level output voltage waveforms, a multilevel inverter has the following advantages:
* If the number of DC bus voltage levels is high, a near-sinusoidal staircase voltage can be generated with only fundamental frequency switching. Fundamental frequency switching minimizes switching losses and is particularly suitable for high power, high voltage applications such as large induction motor drives or static Volt-Ampere reactive (VAr) compensators.
* When the number of levels is sufficiently high, harmonic content will be low enough to avoid the need for filters.
* High voltages on the DC side do not have to be blocked by one switching device only, but by a number of switching devices in series. Therefore, the switching devices in a multilevel inverter can be rated at lower voltages compared to switching devices applied in a full bridge inverter.
* Some multilevel inverter topologies such as the flying capacitor and cascaded multilevel inverters provide switch combination redundancies. These redundancies for example, can be used for balancing the different voltage levels, for minimizing the switching frequency and for employing each switching device equally, hence, avoiding asymmetrical wear and asymmetrical temperature distribution within the inverter.
* Fast dynamic response of a multilevel inverter can be achieved by switching "larger" voltage steps to the output. Due to the flexibility arising from the accessibility of different DC potentials, control schemes can be tailored depending on the application of the inverter [*J. S. Lai* 1996 and *F. Z. Peng* 1996].

Disadvantages of multilevel inverters can be summarized as:
* They require more devices than traditional inverters. The system cost may increase (part of the increased cost may be offset by the fact that switches with lower ratings are being used). Using more devices also means; the probability of a system failure will increase.
* The increased number of switches will result in more complicated control.
* They have narrow range of modulation indexes [*S. Sirisukprasert* 2002].

TRADITIONAL 3-LEVEL VOLTAGE SOURCE INVERTER:

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal AC output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three-phase ac systems. A half-bridge is the simplest topology, which is used to produce a 2-level square-wave output waveform. The full-bridge topology is used to synthesize a 3-level square-wave output waveform. The 3-level full-bridge or H-bridge configuration of the single-phase voltage source inverter is shown in Fig. 1.

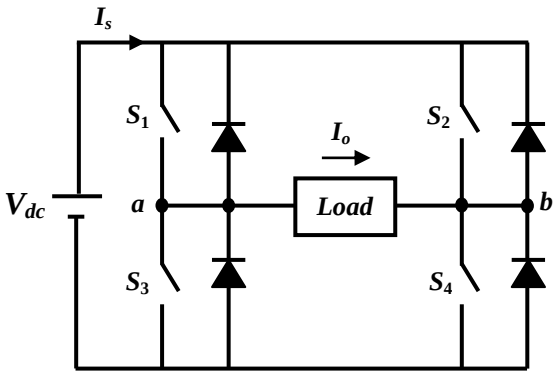

Fig. 1: H-bridge Inverter

The full bridge inverter can provide either Bipolar or Unipolar output voltage switching. The unipolar inverter is optimum for harmonic elimination more than the bipolar inverter. Therefore the unipolar scheme is the optimum technique [*K. S. Krikor* and *J. A. Mohammed* 2002] which is to be compared with the OHESW technique later. The unipolar inverter circuit consists of four main switches and four freewheeling diodes. According to four-switch combination, three output voltage levels, $+V_{dc}$, $-V_{dc}$, and 0, can be synthesized for the voltage across *a* and *b* [*J. M. Jacob* 2004]. Fig. 2 shows the unipolar waveform output from H-bridge inverter.

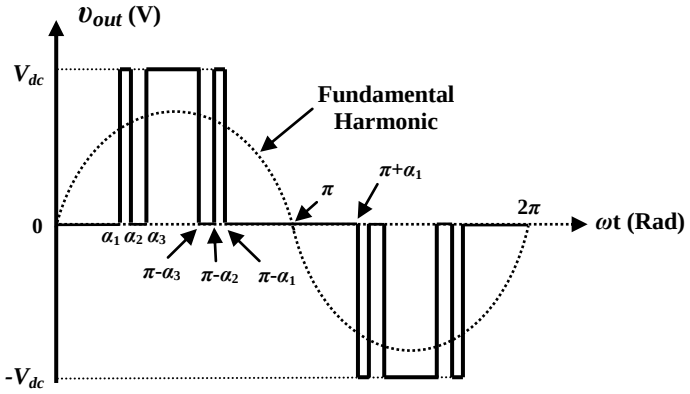

Fig. 2: Unipolar Switching Scheme

- SHEPWM TECHNIQUE:

The SHEPWM technique is currently used to synthesize an output waveform of both a half-bridge and a full-bridge inverter. In this paper, a 3-level SHEPWM generated by a full-bridge inverter is considered.

Since the advent of the family of new semiconductors, tremendous interest has been renewed in inverter technology. The ability of switching devices having turn-off times in the range of a few microseconds or sub microseconds has increased the flexibility of achieving a practically sinusoidal output by employing sophisticated switching patterns in inverter circuit. SHEPWM technique is introduced by *Patel* [*H. S. Patel* 1973]. The idea of such a method is that the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations.

- OPTIMIZED SHEPWM SWITCHING ANGLES:

The optimized unipolar output waveform shown in Fig. 2 is assumed to be the quarter-wave symmetric. *Patel* and *Hoft* [*H. S. Patel* 1973] presented the Fourier series of the 3-level SHEPWM as follows:

$$\upsilon_{out}(\omega t)=\sum_{n=1}^{\infty}\frac{4V_{dc}}{n\pi}\left[\sum_{k=1}^{\infty}(-1)^{(k-1)}\cos(n\alpha_k)\right]\sin(n\omega t) \quad (1)$$

where α_k is the optimized switching angles, which must satisfy the following condition: $0 \le \alpha_1 \le \alpha_2 \le ... \alpha_k \ldots \le \pi/2$. The amplitude of all odd harmonic components including fundamental one, are given by:

$$h_n=\frac{4V_{dc}}{n\pi}\sum_{k=1}^{\infty}(-1)^{(k-1)}\cos(n\alpha_k) \quad (2)$$

where *n* is the harmonic order. The amplitude of DC component and all even harmonics equal zero. Thus, only the odd harmonics in the quarter-wave symmetric waveform need to be eliminated. The switching angles of the waveform will be adjusted to get the lowest output voltage THD.

SOLVING SHEPWM EQUATIONS:

Eqs. 2 are nonlinear equations and transcendental in nature. As a result, many people have utilized numerical iterative techniques in order to solve these equations. For example, *Jian Sun* used the Newton-Raphson numerical technique [*J. Sun* 1992]. Another numerical technique one might use is Gauss-Seidel, although this particular numerical technique is not as robust as Newton-Raphson.
Unfortunately, numerical iterative techniques have their drawbacks:

1. These techniques require an initial guess in order to work. However, if the initial guess is not good enough, a solution will not be found.
2. They will only find one solution, if one exists.
3. They needed large time for calculation. This time increased with increasing the degree of freedom of the nonlinear equations.

The obvious drawback here is that more than one solution might exist to the problem at hand. Using the *fast recursive algorithm* derived in [*D. Czarkowski* 2002]; all solutions to these nonlinear equations can be found without the need for an initial guess.

MULTILEVEL VOLTAGE SOURCE INVERTER:

A multilevel inverter is a power electronic system that synthesizes a desired voltage output from several levels of DC voltages as input, typically obtained from capacitor voltage sources. The so-called "multilevel", starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints.
The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching

frequency or decreasing the inverter power output [*J. S. Lai* 1996]. In this paper, three capacitor voltage synthesis-based multilevel inverters are introduced, i.e.

1. Diode-Clamped Multilevel Inverter.

2. Flying-Capacitor Multilevel Inverter.

3. Cascaded-Inverters with Separated DC Sources [*J. S. Lai* 1996 and *S. Sirisukparsert* 1999].

Implicitly, the multilevel inverter using cascaded-inverters requires the least number of components. Another advantage of cascaded-inverter is circuit layout flexibility. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitor. The number of output voltage levels can be easily adjusted by adding or removing the full-bridge cells.

*** Cascaded H-bridges Multilevel Inverter:**

The cascaded H-bridges multilevel inverter is a relatively new inverter structure [*J. S. Lai* 1996, *T. Cunnyngham* 2001, and *S. M. Tenconi* 1995]. It is proposed here to solve all the above-mentioned problems of the multilevel inverters as well as conventional multi pulse inverters (or traditional PWM inverter). This new multilevel inverter eliminates the excessively large number of *i*) bulky transformers required by conventional multi pulse inverters, *ii*) clamping diodes required by multilevel diode-clamped inverters, and *iii*) flying capacitors required by multilevel flying-capacitor inverters [*F. Z. Peng* 1996].

A cascaded H-bridges multilevel inverter is simply a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter [*J. S. Lai* 1996 and *T. Cunnyngham* 2001].

The cascaded H-bridges multilevel inverter introduces the idea of using (Separate DC Sources) SDCSs to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source V_{dc}. By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced. Fig. 3 provides an illustration of a single-phase cascaded H-bridges multilevel inverter using 3-SDCSs.

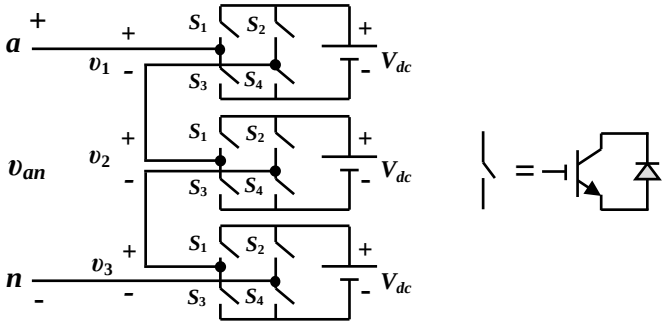

Fig. 3: Cascaded H-bridges Multilevel Inverter using 3-SDCSs

By closing the appropriate switches, each H-bridge inverter can produce three different voltages: $+V_{dc}$, 0 and $-V_{dc}$.

As mentioned earlier, each H-bridge inverter produces an AC voltage v_i, where *i* stands for one particular H-bridge inverter. Fig.3 contains three such H-bridges, one for each DC source. Therefore, to obtain the total AC voltage produced by the multilevel inverter, these three distinct AC voltages are added together.

Fig. 4 provides an illustration of these ideas, when the Multilevel Fundamental Switching (MFS) scheme is used. It also illustrates the idea of "levels" in a cascaded H-bridges multilevel inverter.
The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a 3-level waveform, a single full-bridge inverter is employed.

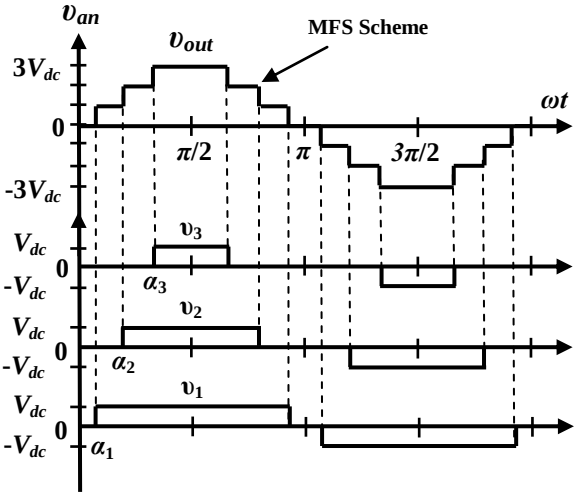

Fig. 4: Output Voltage of Cascaded H-bridges 7-level Inverter

In Fig. 4, one notices that three distinct DC sources (s = 3, where s is the number of DC sources) can produce a maximum of (l = 7 distinct levels) in the output phase voltage of the multilevel inverter. More generally, a cascaded H-bridges multilevel inverter using s-SDCSs can produce a maximum of $2s + 1$ distinct levels l in the output phase voltage [*P. M. Bhagwat* 1983].

OHESW TECHNIQUE:

Among modulation techniques being used these days, OHESW technique is very suitable for multilevel inverter topologies, and low THD output waveform without using any filter circuit is possible.

Basically, the concept of the OHESW technique is to combine the idea of the SHEPWM presented by Patel *et al* [*H. S. Patel* 1973] with the quarter-wave symmetric idea concept presented by Stefano Vic *et al* [*P. M. Bhagwat* 1983]. The concept of the harmonic reduction is presented here to eliminate the specific harmonics, which are the lowest orders.
The proposed technique is to synthesize waveform by the multilevel inverter using cascaded inverter with SDCSs, which was presented in Section A.

OPTIMIZED HARMONIC ELIMINATION SWITCHING ANGLES:

The OHESW is assumed to be the quarter-wave symmetric. Fourier series of the quarter-wave symmetric s H-bridge cell multilevel waveform is written as follows:

$$\upsilon_{out}(\omega t) = \upsilon_{an} = \sum_{n=1}^{\infty} \frac{4V_{dc}}{n\pi} \left[\sum_{k=1}^{s} \cos(n\alpha_k) \right] \sin(n\omega t) \tag{3}$$

where α_k is the optimized switching angles, which must satisfy the following condition: $\alpha_1 < \alpha_2 < ... < \alpha_s < \pi/2$. The amplitude of all odd harmonic components including fundamental one, are given by:

$$h_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \quad (4)$$

where n is the harmonic order. The amplitude of DC component and all even harmonics equal zero. Thus, only the odd harmonics in the quarter-wave symmetric multilevel waveform need to be eliminated. The switching angles of the waveform will be adjusted to get the lowest output voltage THD.

SOLVING OF OHESW EQUATIONS:

When the MFS scheme shown in Fig. 4 is implemented using *s* switching angles, Eq. 4 can be used to derive *s* different harmonic equations. In other words, *s* switching angles will be used to control the values of *s* different harmonics.

Unfortunately, these harmonic equations are transcendental equations, making them difficult to solve without making use of some sort of numerical iterative technique, such as Newton-Raphson.

Until recently, numerical iterative techniques seemed to be the only viable method to solve the aforementioned nonlinear harmonic equations [*P. N. Enjeti* 1990, *H. S. Patel* 1973, and *J. Sun* 1992]. Using Resultant method presented in [*K. S. Krikor* and *J. A. Mohammed* 2007], all solutions (if they exist) to the nonlinear equations can be found without the need for an initial guess. However, by making some simple changes of variables and simplifying, these transcendental equations can be transformed into a set of polynomial equations [*K. S. Krikor* and *J. A. Mohammed* 2007].

RESULTS AND DISCUSSION:

The object of this paper is to design a computer MATLAB program to make comparison between the traditional 3-level inverter with SHEPWM technique and multilevel inverter with OHESW technique, to assist the optimum design calculation, and to get some results such as switching angles (α) necessary for studying the optimum technique.

In the case of SHEPWM scheme, computation was done as the modulation index *m* increased between (0 and 1) and for *K*= (2-17) (*K* is the number switching angles per quarter cycle). The instantaneous SHEPWM, 3-level output voltage waveforms at minimized THD (THDmin) and for *K*=3 and 17, are shown in Fig. 5. A SHEPWM waveform consists of a series of positive and negative pulses of constant amplitude but with variable switching instants. For example, for *K*=3, the 3^{rd} and 5^{th} harmonics will be eliminated from the output voltage waveform. Increasing *K* causes increasing the number of odd harmonics to be eliminated.

In the case of OHESW scheme, computation was done as *m* increased between (0 and *s*) and for number of voltages levels *l* = (5-15). Fig. 6 shows the instantaneous output voltage OHESW for two values of voltage levels (*l* = 7 and 15) and with THDmin. If the number of *l* is higher, a near-sinusoidal staircase voltage can be generated with only fundamental frequency switching.

The optimization technique has been used to minimize the harmonics content of the inverter output voltage. The best compromise between efficiency and quality of the inverter operation is achieved by the optimal switching pattern technique [*K. S. Krikor* and *J. A. Mohammed* 2002].

The behavior of the motor drive is explained by the simulation program. By using the equivalent circuit of the motor and the corresponding performance equations, it can be easy to analyze the performance of the motor operated on an inverter under the proposed two techniques.

Fig. 7 illustrates the comparison of the proposed motor drive performance under the SHEPWM and OHESW techniques to get the optimum one. From the figure, it can be seen that the THD, switching losses Psw_{min}, additional motor power losses $\Sigma Padd_{min}$, and additional motor pulsating torque $Tpulsadd_{min}$, motor current I_{rmin} and motor input power Pin_{min} versus K are less with OHESW technique than that with SHEPWM technique. On the other hand, the optimum technique should maximize the motor power factor Pf_{max} and efficiency η_{max} for same K. These factors for OHESW scheme seem to be higher than with SHEPWM scheme.

THD curve shows that THDmin increases with K for SHEPWM technique while it decreases with K in the case of OHESW technique. On the other hand THDmax decreases with K in the two techniques [See also Table 1]. It can be seen from the figure, that the motor performance with OHESW technique is approximately constant with K or $s > 3$ ($l > 7$), and converges form that motor performance which excited from pure sinusoidal excitation while, it does not converges to that performance with increasing K, in the case of SHEPWM technique [See also Table 2]. Therefore the cascade multilevel with 7-level is suitable to get good performance of the proposed motor with less cost [All the motor parameters are listed in Table 3 in the Appendix].

From the simulation results, THDmin of the 15-level, or 7-switching ($s = K = 7$), OHESW waveform is 6.4554 % with modulation index $m_a = m/s = 0.7036$ [See Table 1], when each power switch is switching one time per cycle (50Hz) for single-phase cascade multilevel inverter, which may can meets the 5% of IEEE standard for the three-phase multilevel inverter without any filter circuits. On the other hand, THDmin of the 7-switching, SHEPWM waveform is 49.1002 %, with $m_a=0.79$, (which does not decrease with increasing K like OHESW does) and each power switch is switching 28 times per cycle (1.4 kHz). As a result THD in OHESW decreased by 86.85 % and the switching losses decreases 28 times with respect to SHEPWM waveform. It can also be seen that for the same output power $Pout_{min}$, the inverter under the OHESW control exhibits less switching losses than that under SHEPWM control, for example; with $Pout_{min}$= 175.1732Watt, the multilevel inverter needs 3-switching angles per quarter cycle ($K = s = 3$) while traditional 3-level inverter needs approximately 9-switching ($K = 9$).

As a result, the waveform under OHESW control for multilevel inverter is apparently closer to a sinusoidal waveform and has less harmonic content, less switching losses, reduced voltage stress on each power device, as a result, higher quality power and higher efficiency than the waveform under SHEPWM control for traditional 3-level inverter. Therefore, multilevel inverter is better than the traditional 3-level PWM inverter of improving waveform quality.

CONCLUSIONS:

The multilevel inverter topology can overcome some of the limitations of the standard 2-level or 3-level inverter. Output voltage and power increase with number of inverter levels.

Harmonics decrease as the number of levels increase. In addition, increasing multilevel output voltage does not require an increase in voltage rating of individual force commutated devices.

In OHESW multilevel inverter, not only does the line voltage THD decrease, but also the lowest exist harmonics is shifted to higher frequency. This, size of a filter circuit applied in OHESW inverter can be decreased dramatically.

Traditional Pulse Width Modulation (PWM) methods employ switching frequencies on the order of several kHz, while Multilevel Fundamental Switching (MFS) scheme employs 50Hz. Therefore, this scheme will lead to minimum switch conduction losses comparable to typical PWM schemes. However,

switching losses increase as the switching frequency increases. As a result, it is desirable to make the switching frequency as low as possible.

The comparative results show that the OHESW technique for multilevel inverter is the optimum technique for improving the quality of the motor drive. Therefore, the best compromise between efficiency and quality of operation is achieved by the multilevel inverter.

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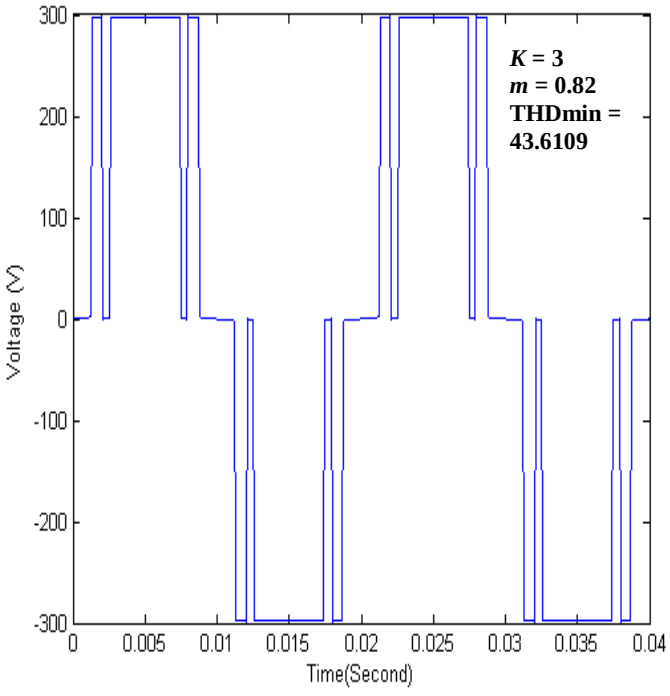


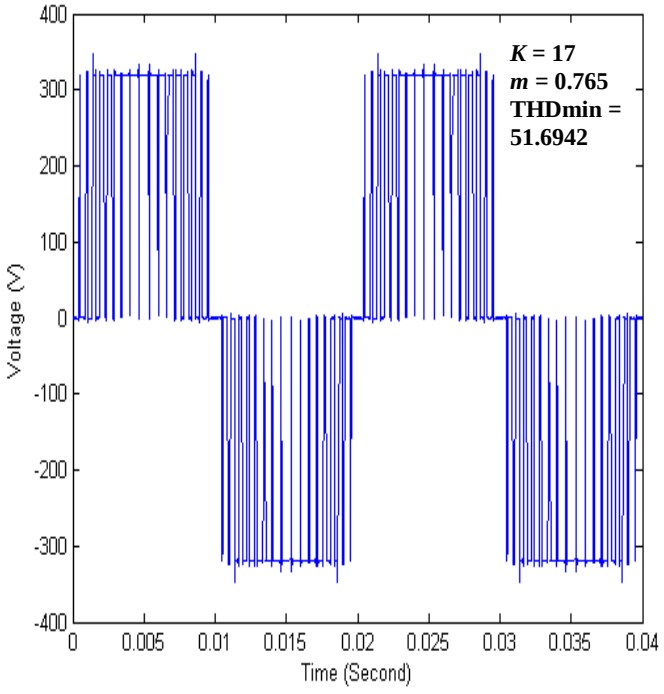


Fig. 5: the Instantinuos Voltage of SHEPWM 3-Level Inverter at THDmin with Different No. of Switching Angles (*K*)

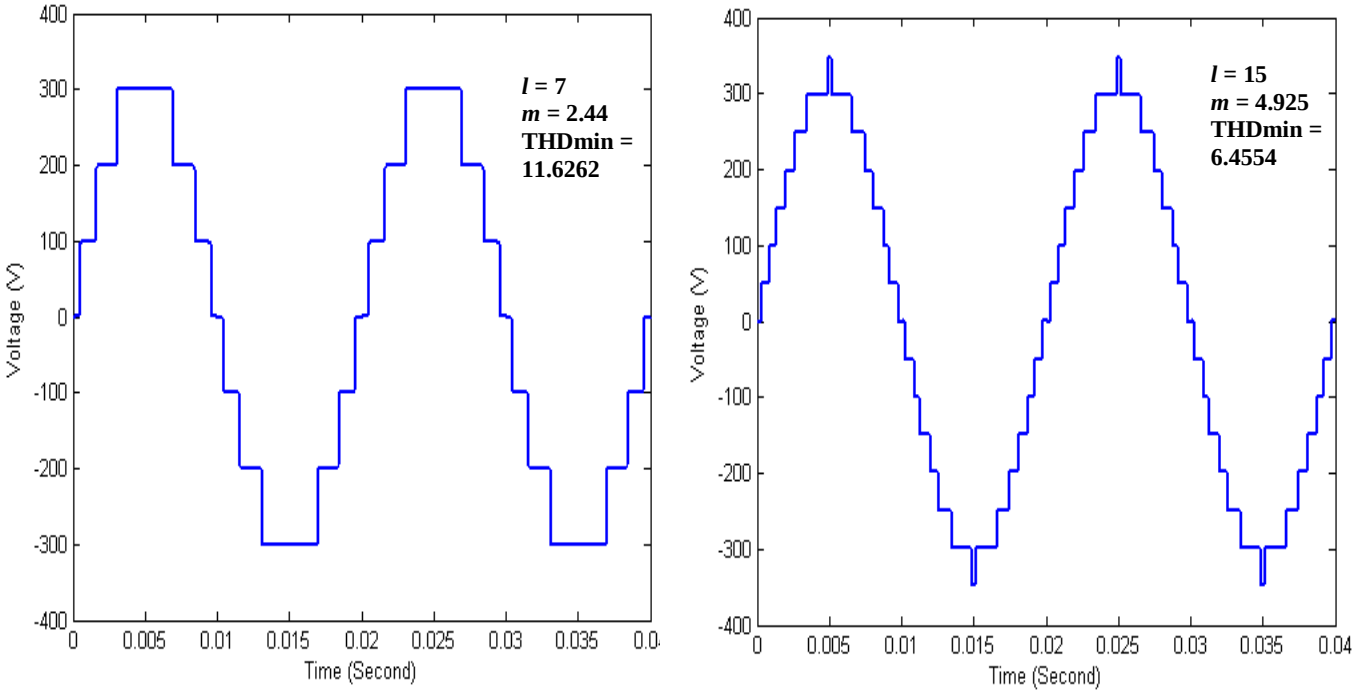
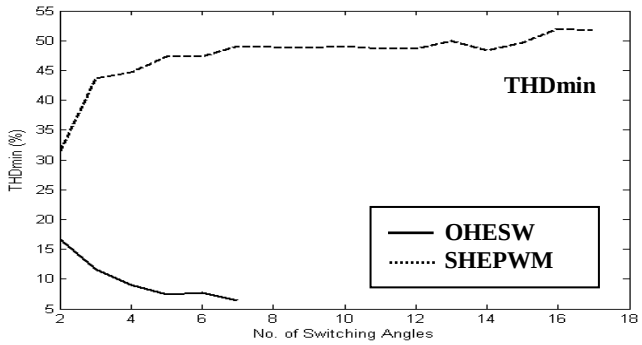
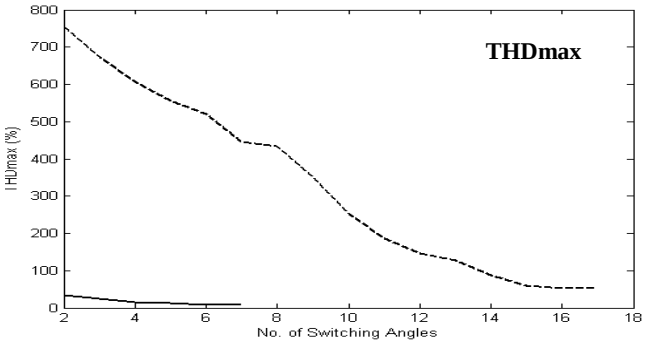
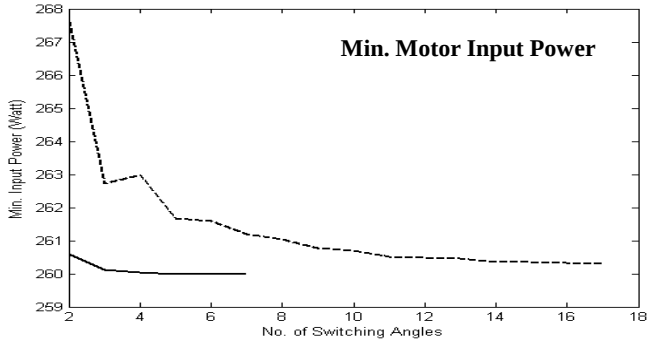
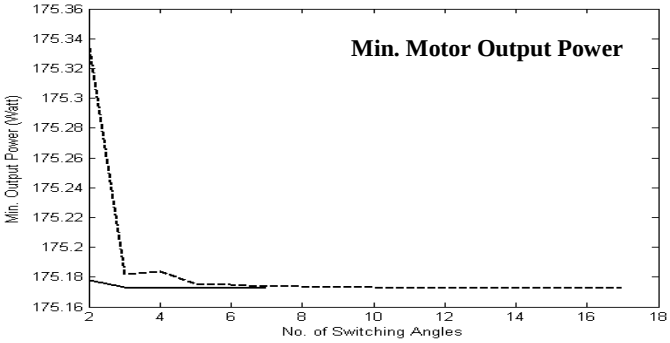


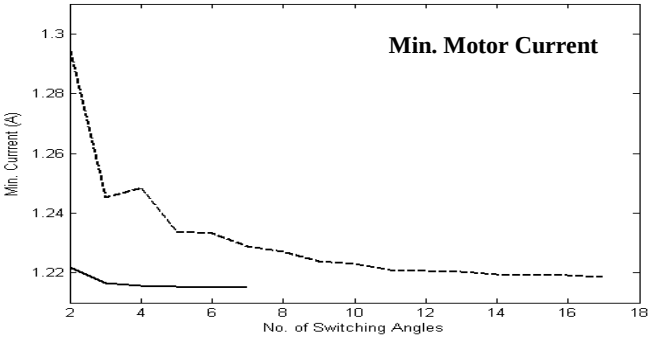
Fig. 6: The Instantaneous Voltage of OHESW Multilevel Inverter at THDmin with Different Voltage Levels (*l*)

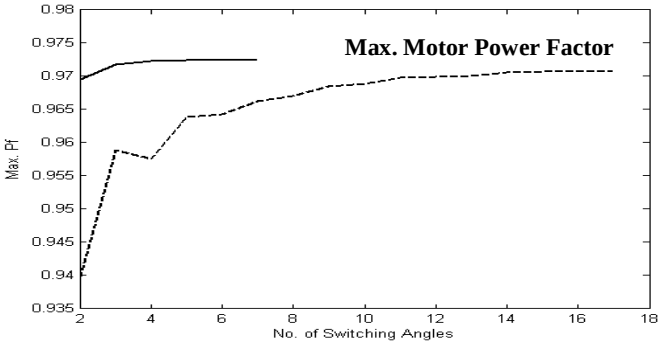

THDmin
THDmin (%)
OHESW
SHEPWM
No. of Switching Angles

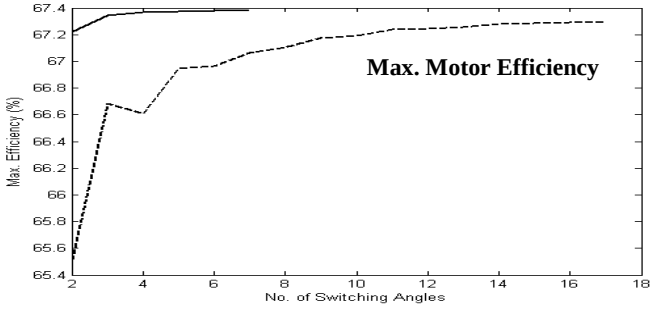

THDmax
THDmax (%)
No. of Switching Angles

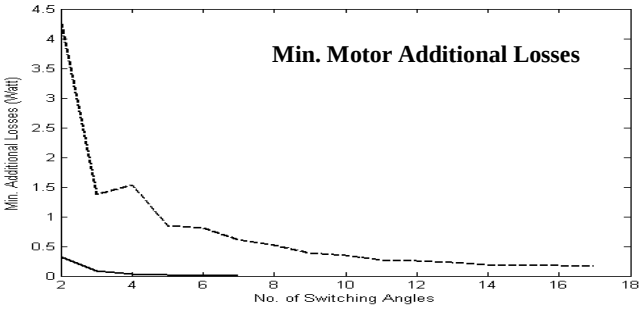

Min. Motor Input Power
Min. Input Power (Watt)
No. of Switching Angles

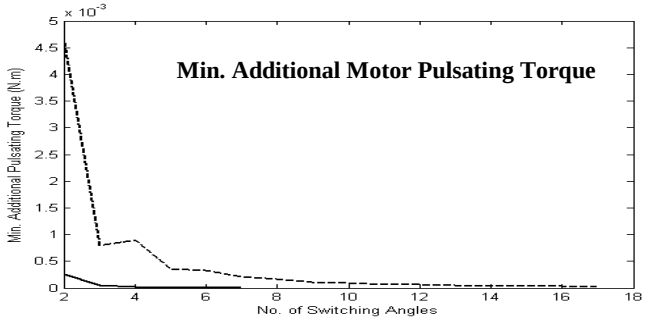

Min. Motor Output Power
Min. Output Power (Watt)
No. of Switching Angles


Min. Motor Current
Min. Current (A)
No. of Switching Angles


Max. Motor Power Factor
Max. Pf
No. of Switching Angles


Max. Motor Efficiency
Max. Efficiency (%)
No. of Switching Angles


Min. Motor Additional Losses
Min. Additional Losses (Watt)
No. of Switching Angles


Min. Additional Motor Pulsating Torque
Min. Additional Pulsating Torque (N.m)
No. of Switching Angles

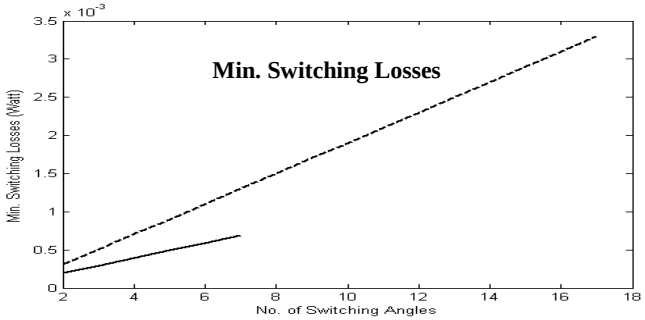

Min. Switching Losses
Min. Switching Losses (Watt)
No. of Switching Angles

Fig. 7: Comparison of Performance between Motor Drive Multilevel Inverter and Traditional 3-level Inverter with Different *K*

APPENDIX

Table 1: the Optimum Performance of the Motor Drive Fed by OHESW Multilevel Inverter

No. of Levels *l*	5	7	9	11	13	15
m	1.67	2.44	3.22	4	4.15	4.925
THD_{min} (%)	16.5924	11.6262	8.9907	7.3873	7.6396	6.4554
THD_{max} (%)	32.9620	24.8098	14.6081	12.1832	9.1754	7.5029
I_{rmin} (A)	1.2218	1.2167	1.2156	1.2153	1.2152	1.2150
$\Sigma Padd_{min}$ (W)	0.328	0.08	0.0322	0.0169	0.0122	0.0071
Pin_{min} (W)	260.5941	260.1219	260.0283	259.9978	259.9887	259.9784
$Pout_{min}$ (W)	175.1772	175.1732	175.1726	175.1725	175.1725	175.1725
η_{max} (%)	67.2225	67.3427	67.3668	67.3746	67.377	67.3796
Pf_{max}	0.9695	0.9718	0.9723	0.9725	0.9725	0.9726
$Tpulsadd_{min}$(N.m)	2.5464e-4	4.8729e-5	1.6782e-5	7.7663e-6	4.3794e-6	2.3517e-6
Psw_{min}* e-4 (W)	1.9784	2.955	3.9366	4.9194	5.9028	6.8859

Table 2: The Optimum Performance of the Motor Drive Fed by SHEPWM Traditional 3-level Inverter

Switching No. (*K*)	2	3	4	5	6	7	8	9
m	0.86	0.82	0.81	0.8	0.8	0.79	0.79	0.79
THD_{min} (%)	31.5599	43.6109	44.6251	47.2747	47.3379	49.1002	48.9801	48.803
THD_{max} (%)	754.8863	671.5544	607.9097	555.3122	521.5931	446.6963	433.3106	352.5778
I_{rmin} (A)	1.2943	1.2453	1.2484	1.2339	1.2331	1.2288	1.227	1.2239
$\Sigma Padd_{min}$(W)	4.2568	1.3808	1.5275	0.8425	0.8029	0.6061	0.5254	0.3889
Pin_{min} (W)	267.6173	262.7127	262.9976	261.6739	261.596	261.2057	261.0438	260.7677
$Pout_{min}$ (W)	175.3341	175.1819	175.1836	175.1754	175.1751	175.1739	175.1735	175.1730
η_{max} (%)	65.5167	66.6819	66.6103	66.9442	66.964	67.0636	67.105	67.1759
Pf_{max}	0.9398	0.9589	0.9576	0.9639	0.9643	0.9663	0.9671	0.9685
$Tpulsadd_{min}$ (N.m)* e-4	46	7.925	9.024	3.6273	3.3608	2.1619	1.741	1.1174
Psw_{min} (W)	3.1437e-4	5.0410e4	7.0749e4	8.991e-4	0.0011	0.0013	0.0015	0.0017

Con. Table 2

Switching No. (*K*)	10	11	12	13	14	15	16	17
m	0.79	0.79	0.79	0.78	0.79	0.78	0.765	0.765
THD_{min} (%)	49.0488	48.7001	48.6333	50.0234	48.3048	49.6866	51.9878	51.6942
THD_{max} (%)	251.9755	185.042	146.6671	128.137	88.6293	59.0839	51.9878	51.6942
I_{rmin} (A)	1.2231	1.221	1.2208	1.2204	1.2194	1.2191	1.2191	1.2186
ΣP_{addmin}(W)	0.3521	0.2638	0.2532	0.2361	0.1909	0.1814	0.1784	0.1586
Pin_{min} (W)	260.6928	260.5125	260.4908	260.4559	260.3626	260.3431	260.3373	260.2961
$Pout_{min}$ (W)	175.1729	175.1727	175.1727	175.1727	175.1726	175.1726	175.1726	175.1725
η_{max} (%)	67.1952	67.2416	67.2472	67.2562	67.2802	67.2853	67.29	67.3
Pf_{max}	0.9689	0.9698	0.9699	0.9701	0.9706	0.9707	0.9707	0.9709
$Tpulsadd_{min}$* e-4 (N.m)	0.96199	0.62763	0.58992	0.51879	0.38868	0.3519	0.33021	0.27785
Psw_{min} (W)	0.0019	0.0021	0.0023	0.0025	0.0027	0.0029	0.0031	0.0033

Table 3: Parameters and Specifications of the Proposed Motor

Turn ratio	a_s	1.066	
Number of pole pair	P	2	
Main winding resistance	R_{1m}	33.5	Ω
Main winding leakage reactance	X_{1m}	27	Ω
Auxiliary winding resistance	R_{1a}	34.5	Ω
Auxiliary winding leakage reactance	X_{1a}	28	Ω
Rotor resistance	R_2	20	Ω
Rotor leakage reactance	X_2	12.5	Ω
Magnetization reactance	X_m	173	Ω
Rated supply voltage	V_1	220	V
Rated current	I	1.215	A
Total Power losses	ΣP	85	W
Output power	P_2	175	W
Efficiency	η	67.38	%
Power factor	P_f	0.9726	
Rated speed	N_r	1275	Rpm
Capacitance	C	6	μF