DESIGN & IMPLEMENTATION OF FRACTIONAL – N FREQUENCY SYNTHESIZER

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ABSTRACT

This research involves design & implementation of fractional – N frequency synthesizer with the following specifications: Frequency range (2350– 2750) MHz,Step size (1 kHz), Switching time 8.9 µs, & phase noise @10 kHz = -115dBc & spurious -69 dBc

The third order Fractional –N technique was chosen to satisfy the design requirements. In this system the ΣΔmodulator placed on digital phase-locked loop to control the fractional value of the frequency division ratio thereby eliminating spurious and allowing good phase noise performance. The development in I.C. technology provides the simplicity in the design of fractional –N frequency synthesizer because it implements the phase frequency detector(PFD) , prescalar, ΣΔmodulator & reference divider in single chip. Therefore our system consists of a single chip contains (low phase noise PFD, charge pump, prescalar, ΣΔmodulator & reference divider), voltage controlled oscillator , loop filter & reference oscillator.

The application of this synthesizer in frequency hopping systems, wireless transceivers ,GSM & radar because it has high switching speed ,low phase noise & low spurious level.

يصف هذا البحث تصميم وبناء مركب ترددات من نوع (Fractional - N) وبالمواصفات التالية : مدى الترددات الخارجة (2350–2750) ميكا هرتز، واقل سعة قفزة 1كيلو هرتز ،زمن تحويل 8.9مايكرو ثانية ومستوى ضوضاء طوري – 115. ديسبيل عند 10000 هرتز من التردد الخارج.ومستوى الطفيليات – 69 ديسبيل.ان تقنية الجيل الثالث (Fractional - N) تم اختيارها لتحقيق متطلبات التصميم. في هذه المنظومة , مرحلة تضمين من نوع (ΣΔ) تم وضعها في دائرة إقفال الطور الرقمية للسيطرة على على القيم الكسرية لمقسم التردد.وبهذا تم ابعاد الترددات الطفيلية وتحسين ضوضاء الطور.

التطور الحاصل في الدوائر المتكاملة جهز البساطة في تصميم مركب الترددات من نوع (Fractional - N) وذلك لأنه دمج كاشف التردد والطور ,ومقسم التردد الثنائي , ومقسم التردد ومرحلة تضمين من نوع (ΣΔ) في شريحة رقيقة واحدة. لذلك منظومتنا تتكون من شريحة تحتوي على كل من (كاشف ترددات وطور ذو ضوضاء طوري قليل،مضخة شحنة دقيقة،مقسم ترددات مبرمج ، ومقسم تردد ثنائي(p/(p+1)) مبرمج ومرحلة تضمين من نوع (ΣΔ)) مرشح ترددات واطئة ،مذبذب ترددات ذو سيطرة جهدية، ومذبذب مرجعي. هذه الشرحة الرقيقة التي تحتوي كل من كاشف ترددات وطور مقسم ترددات مبرمج ومقسم تردد ثنائي .

التطبيقات لهذا المركب في منظومات القفز بالتردد , و الرادار, و المرسلات والمستلمات اللاسلكية،GSM وذلك لأنها تمتلك خاصية ضوضاء طوري قليل وسرعة تحويل عالية ومستوى طفيليات اقل.

KEY WORDS
Fractional- N, ΣΔ modulator, PLL(phase lock loop)

INTRODUCTION

Fractional –N was originally developed 31 to 36 years ago then called Digi-phase and later Fractional –N by Racal and H.P.[Li, Lin, 2000].there are three types of fractional-N technique. In the first order technique , the fractional division can be used to increase the reference by an order of magnitude or to reduce the division ratio. The first order appears to be solution to the drawbacks of PLL ,but this type has not been the case. Naturally , fractional division generates a new periodicity within the Division by N and therefore, introduces spurious signals. An improvement can be achieved by analogue compensation of the phase error. The phase error exactly represents by the content of the accumulator. This allows to cancel the spurious. The analogue compensation represents the second order. But it has disadvantage in accuracy. An alternative to the second order is the third order fractional-N, it uses all digital spurious cancellation by implementing sigma-delta modulation.

A general rule and requirement in PLL designs to try to use the highest-frequency reference and the lowest division ratios. Also, the higher-frequency reference is easier to
filter out and yields a lower division ratio, which produces better phase noise, lower spurious signal response, and better switching time. However, in many cases these requirements conflict with the rest of the design parameters, since high resolution (fine step size) requires low reference frequency and therefore high division ratios. If the reference frequency is high, then the frequency resolution or the step size is high. To achieve small step size, it is necessary to either use low reference frequencies or resort to multiloop designs. This increases the complexity, size, and cost. All the designs that we demonstrated assumed the divider ratio *N* to be a whole number. But if *N* could include a
whole number plus a fraction, it would be possible to generate step sizes that are smaller than the reference frequency. The fractional N frequency synthesizer is a modified version of the PLL based synthesizer where the integer frequency divider is replaced by a fractional frequency divider. **Fig. (1)** shows the simplified block diagram of a fractional N synthesizer. The only difference from the PLL based synthesizer is that the frequency divider has a choice between two integers, *N* and *N+1*.

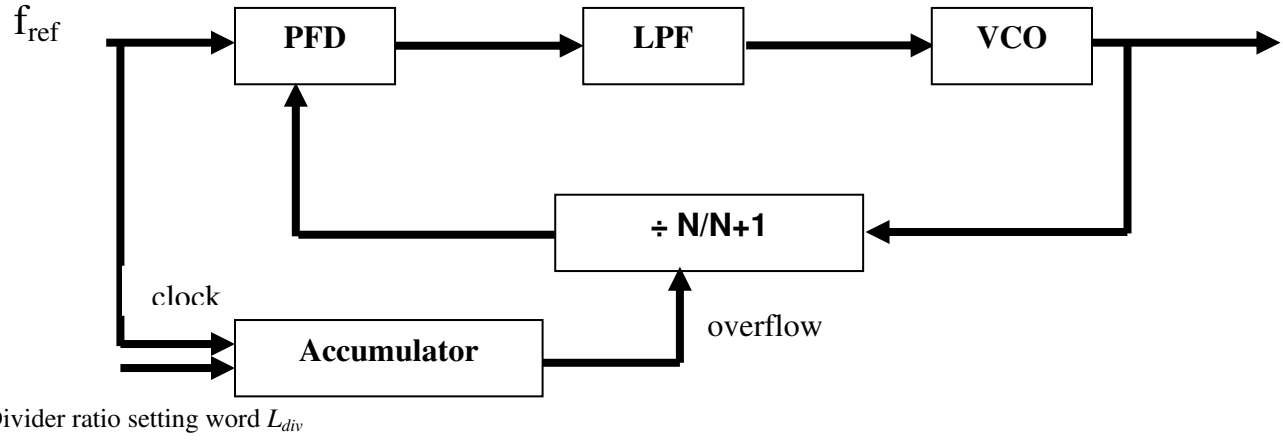

Fig. (1): Fractional N frequency synthesizer block diagram

The reference clock also provides the clock signal for the phase accumulator. The phase accumulator accumulates its output with a divider ratio setting the word of length L_{div} at each clock cycle. The dual-mode divider divides its input by N when the phase accumulator is not overflowed. When an overflow signal from the phase accumulator appears, the dual-mode divider divides its input by $N+1$. On average, the divider divides its input by a fractional value between N and $N+1$. To calculate the exact divider ratio, we assume the accumulator length to be L_{acc}. For every L_{acc} clock cycles, the accumulator overflows L_{div} times. That means for every L_{acc} clock cycles, the divider divides its input by $N+1$ L_{div} times, and divides by N for the rest of the times. If N_{avg} is the average dividing ratio, then

$$N_{avg} L_{acc} = N (L_{acc} - L_{div}) + (N + 1) L_{div} \quad eq(1.1)$$

And

$$N_{avg} = N + L_{div}/L_{acc} \quad eq(1.2)$$

The fractional divider ratio makes it possible to have a much smaller frequency step with the same reference frequency comparing to the PLL based synthesizer. In other words, the fractional N synthesizer can have a higher reference frequency and hence higher loop bandwidth without compromising the stability of the loop. But the fractional divider ratio is achieved through an averaging process. The alternating N, $N+1$ divide numbers cause the output frequency to vary between $N*f_{ref}$ and $(N+1)*f_{ref}$.

ADVANTAGES & DISADVANTAGES OF FRACTIONAL N SYNTHESIZER

In a fractional-N phase-locked loop, the division ratio N is switched between two or more integer values in such a way that the *average* value of N can be a fractional number. Consequently, the phase comparison frequency can be much higher than in integer-N synthesizers, and thus the division ratio can be much lower. For example in the DCS-1800 system, a phase comparison frequency of 13 MHz would result in N ranging from 131 to 145. A channel spacing of 200 kHz then requires the ability to change the division ratio in steps of $200/13000 \approx 0.0154$[Conkling, Craig , Feb,1998].

A reference frequency of 13 MHz, or 65 times higher than in the integer-N synthesizer, also (theoretically) enables up to 65 times higher loop bandwidth. This in turn results in up to 65 times faster switching. In practice, however, the maximum loop bandwidth is limited by factors other than the reference feedthrough, and cannot be increased as much. Still, the designer now has more freedom in choosing the loop bandwidth. If, for example, a very good reference suppression is required, the loop bandwidth can be made significantly smaller while still meeting the switching time requirements. In short, using a fractional-N PLL instead of an integer-N one loosens the coupling between the choice of loop bandwidth and the choice of the reference frequency.

Also, since the division ratio is smaller than in integer-N synthesizers, the phase noise of the reference oscillator is not amplified as much. In the above example, the reference frequency was increased from 200 kHz to 13 MHz. This reduces the amplification of the crystal oscillator phase noise in the DCS-1800 system from 40dB to 22dB.

The main source of problems in fractional-N synthesizers is the fact that although the *average* division ratio is a fractional number, the *instantaneous* division ratio must still always be an integer. In practice, the fractional division is typically performed by using an accumulator, i.e. a digital adder that adds a fraction F of its full scale value to its contents once every reference clock cycle. During the accumulation, the prescaler divides its input frequency by N. Every time the accumulator overflows, the prescaler divides by $N+1$ for one cycle. The average output frequency will now be

$$f_{out} = (N + F) f_{ref} \quad eq(2.1)$$

During the accumulation, the divided VCO frequency seen at the phase detector input is

$$f_{vco} = f_{ref} + (F/N) f_{ref} \quad eq(2.2)$$

On the other hand, the reference frequency seen at the other phase detector input is always *fref* . Thus, the phase error at the input of the phase detector increases at a rate of

$$\Delta\theta_e(t) = 2\pi\ (F/N)\ (t/T_{ref}) \qquad \text{eq(2.3)}$$

When an overflow occurs in the accumulator, the prescaler divides by N+1 for one period, corresponding to a 2π decrease in the phase error at the phase detector input. The resulting phase error has a sawtooth shape. The sawtooth shaped phase error, also known as a "beat note", causes spurious tones in the output spectrum at offsets of $\pm K \cdot F \cdot fref$, where $K = \{0, 1, 2\ldots\}$, i.e. at integer multiples of $F \cdot fref$. These spurious tones, having a large energy in a very small bandwidth, are well as the phase noise of the PLL, causing significant problems in almost all applications. What magnifies the problem is the fact that spurs occur at fractional multiples of *fref*, i.e. they can occur well within the channel bandwidth, and inside the PLL bandwidth as well.

SPUR CANCELLATION TECHNIQUES

Only the very first implementations of the fractional-N divider operated as above. The spurious tones limit the performance of the synthesizer so much that it is practically unusable in most applications. Different methods to eliminate the sawtooth phase error, and thus the spurs. These methods will be discussed in the following subsections.

Analog compensation

The first proposed means of correcting the sawtooth phase error was injecting an opposite ramp signal somewhere in the loop so that the sawteeth cancel each other. In the first order fractional-N synthesizer, the synthesizer has two identical digital accumulators, one controlling the prescaler modulus, and the other one controlling a "sideband reduction circuit". The sideband reduction circuit generates a sawtooth signal with an opposite polarity than the sawtooth at the input of the phase detector. This correction signal is then added to the VCO control voltage node. Ideally, the VCO control voltage is now constant when the loop is in lock. In this method , precision analog components are needed[j. Craeninkx & M. Steyaert, 1998].

Sigma delta modulation

This method will be used to implement fractional N synthesizer in my system to eliminate the fractional spurs. The basic principles of the digital ΣΔ modulation will be presented in the following.

Fundamentals

The accumulator used to control the modulus of the prescaler can be viewed as the digital counter part of a first-order analog ΣΔ-modulator. The carry of Accumulator changes the prescalar from N to N+1 for one cycle **Fig. (3.1)** shows the accumulator, i.e. an adder with a one clock cycle delay in the feedback path, with the corresponding signals. The frequency control word is fed into the *A* input, and added to the *B* input to produce a sum output Σ. When the adder overflows, the carry out bit *c* is set[Goldberg, Bar-Giora , 1999].

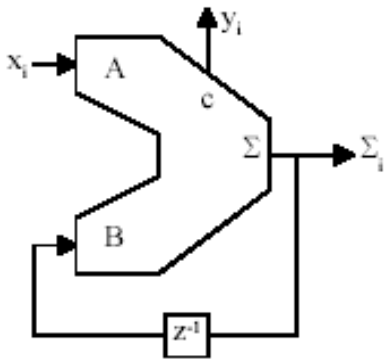

Fig. (3.1) The digital accumulator with the corresponding input and output signals.

Let us denote the frequency control signal fed to input *A* by *xi*, and carry output *c* of the accumulator by *yi*. When an overflow occurs, the contents of the accumulator are "flipped over", which can be viewed as subtracting the full scale of the accumulator from its contents.
The output of the accumulator at an arbitrary time is the sum of its input at that time and its contents one clock period earlier. If an overflow occurs, the full scale of the accumulator is subtracted. The output can thus be expressed as

$\Sigma_i = x_i + \Sigma_{i-1} - y_i$ eq(3.1)

$y_i = x_i + \Sigma_{i-1} - \Sigma_i$ eq(3.2)

$y_i = x_i - (\Sigma_i - \Sigma_{i-1})$ eq(3.3)

The z-transform of equation (3.3) is

$Y(z) = X(z) - \Sigma(z)(1 - z^{-1})$ eq(3.4)

Let us now look at the signal flow diagram of a first-order analog ΣΔ-modulator shown in **Fig. (3.2)**. The input is again denoted by *x*, and the output by *y*. The operation performed in the dashed box is the quantization, and *e* denotes the quantization error.

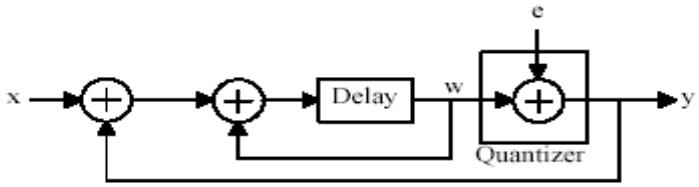

Fig. (3.2) The signal flow diagram of a first-order analog ΣΔ-modulator.

The above modulator is described by the following equations:

$w_i = w_{i-1} + x_{i-1} - y_{i-1}$ eq(3.5)

$y_i = w_i + e_i$ eq(3.6)

Combining these two, we get

$y_i - e_i = y_{i-1} - e_{i-1} + x_{i-1} - y_{i-1}$ eq(3.7)

$y_i = x_{i-1} + e_i - e_{i-1}$ eq(3.8)

The z-transformation of Equation (3.8) is

$Y(z) = z^{-1} X(z) + E(z)(1 - z^{-1})$ eq(3.9)

Comparing Equation (3.9) with Equation (3.4) shows great similarity. Ignoring the latency of one clock period in the signal path of the analog ΣΔ-modulator, and treating the contents of the digital accumulator as the negative of the quantization error, the equations are identical.
A ΣΔ-modulator shapes the quantization noise in a high pass fashion. In other words, the quantization noise is pushed to higher frequencies, and the signal-to-noise ratio at low frequencies can be very high. **Fig. (3.3)** shows the output spectrum of an analog first order ΣΔ-modulator with a low frequency input[Dean banerjee , 2005].

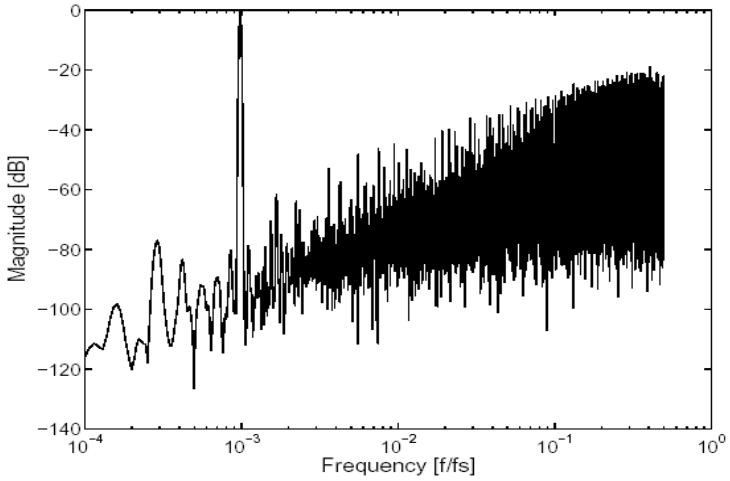

Fig. (3.3): The output spectrum of an analog ΣΔ-modulator with a low-frequency input signal.

Looking at **Fig. (3.3),** it would seem that the quantization noise is originally white, and then shaped into higher frequencies. The white noise assumption, however, holds only for "sufficiently busy" input signals. In fractional-N synthesizers, the input signal is normally constant, and the quantization noise is no longer white. The quantization noise power is concentrated into a finite number of spurious tones. The spurious performance combined with the relatively poor noise shaping (20dB/decade) make the first order ΣΔ-modulator quite useless in practical applications.

Cascaded (MASH) modulators

As explained above, the spurious tones at the output of the modulator result from the input being DC. The signal in the ΣΔ-output of the accumulator, however, is no longer at DC, although it is periodical. Now, this signal can be fed into the input of another accumulator, whose output will be much less periodic than the output of the first accumulator. The first accumulator carry changes the division ratio of the Divider from N to N+1 for one cycle. The output is digitally integrated by the second accumulator and its carry output changes the division ratio to N+1 and then N-1 on the next clock cycle. Combining the *c* outputs of the two accumulators in a suitable way(see **Fig (3.4),** the quantization noise of the first accumulator can be canceled[J.A Crawford , 1994].

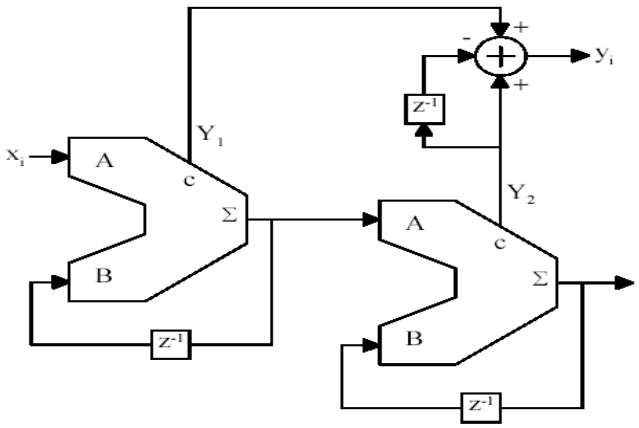

Fig. (3.4): The block diagram of a second-order MASH modulator.

As shown in Equations (3.1) to (3.4), the output of the first accumulator is

$Y(z) = X(z) - \Sigma_1(z)\,(1 - z^{-1})$ eq(3.10)

Feeding the Σ -output of the first accumulator into the input of the second one, the output of the second accumulator is

$Y_2(z) = \Sigma_1(z) - \Sigma_2(z)\,(1 - z^{-1})$ eq(3.11)

Combining the outputs of the accumulators as shown in Figure 3.4, we get the following as the output of the entire modulator:

$Y(z) = Y_1(z) + Y_2(z) - Y_2(z)\,z^{-1}$ eq(3.12)

$Y(z) = Y_1(z) + Y_2(z)\,(1 - z^{-1})$ eq(3.13)

$Y(z) = X(z) - \Sigma_1(z)\,(1 - z^{-1}) + \Sigma_1(z)\,(1 - z^{-1}) - \Sigma_2(z)\,(1 - z^{-1})^2$ eq(3.14)

$Y(z) = X(z) - \Sigma_2(z)\,(1 - z^{-1})^2$ eq(3.15)

As Equation (3.15) shows, the quantization noise of the first accumulator cancels out. This greatly improves the spurious performance of the modulator, since the first accumulator is the one with the more periodical output. Also, as Equation (3.15) shows,
the noise transfer function is now a second-order high pass function. Thus, the signal to noise ratio at low frequencies is higher than in a first-order modulator.

This concept, called the cascaded modulator or the MASH modulator, MASH modulators of any order are unconditionally stable if individual modulators comprising the MASH are stable. In this case, the individual modulators are first-order ones, and thus always stable. Hence, the order of the MASH modulator can be increased at will without causing any stability problems. In the case of three accumulator or more, the third accumulator changes the prescalar to N+1,N-2,N+1,the fourth uses the sequence N+1,N-3,N+3,N-1, and the more sequence will be shown in **Fig. (3.5)**. As shown in figure (3.5), the sequence forms a Pascal triangle but with the overall sum of each row being zero with exception of the output from the first accumulator. Hence the second and subsequent accumulators have no long term effect on the division ratio[Mike Curtin and Paul O'Brien, 1999].

In digital ΣΔ-modulators, increasing the order of the modulator improves the spurious performance and the low-frequency SNR basically unrestrictedly. However, a higher order noise transfer function of the modulator causes problems in the design of the loop filter. The quantization noise of the modulator is pushed to higher frequencies, and rises with frequency at a rate of 20 decibels per decade per modulator order. For example, the quantization noise of a third-order modulator rises at a rate of 60 dB/decade[Li Lin , 2000].

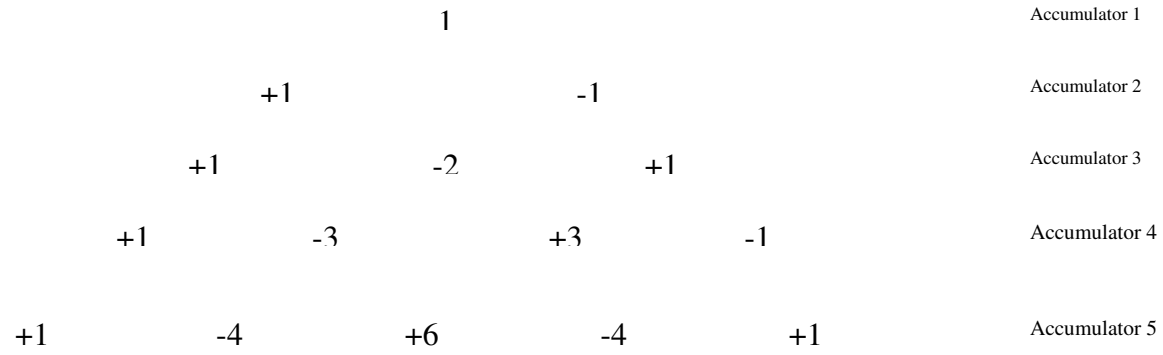

Fig. (3.5): Pascal's triangle

SYSTEM DESIGN

Based on theoretical analysis shown in section three a fractional –N synthesizer will be designed for the following requirements :

- Frequency range : 2450 MHz – 2750 MHz

- Step size : 1kHz
- Switching speed : less than 10 µsec
- Phase noise : less than -80dbc/Hz @ 10 kHz
- Spurious : -60 dB

The sigma delta modulator will be used to implement the system since it has the following properties:

- eliminating spurious digitally.
- Allowing good phase noise performance.

The sigma delta modulator in this system contains four stage of accumulator. The system contains on the following parts as shown in the schematic diagram**Fig. (4.1).**

- Single chip : contains phase frequency detector , charge pump , N-divider & ΣΔ-modulator.
- Voltage controlled oscillator.
- Loop filter.
- Frequency oscillator.

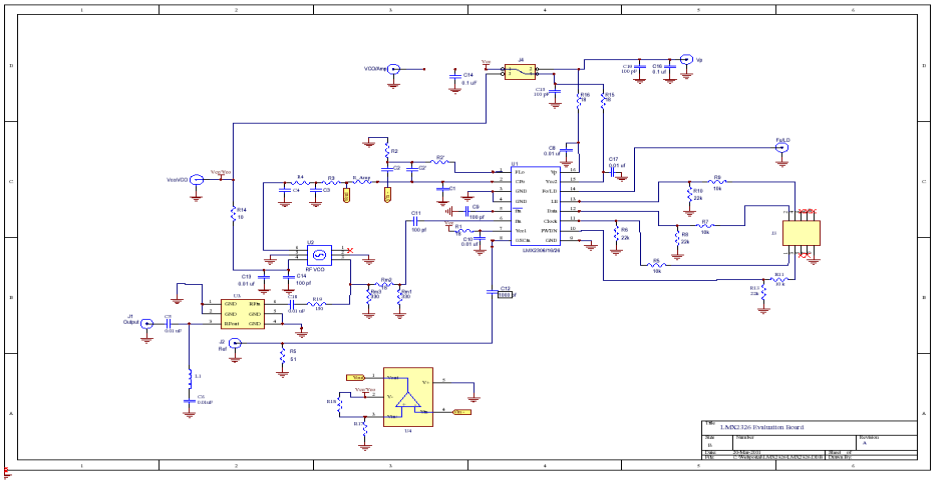

Fig. (4.1): Schematic Diagram

Single chip (LMX2486)

The LMX2486 consists of low phase noise phase frequency detector(PFD) ,N counters, R counters, ΣΔ-compensation and charge pump. The LMX2486 is fabricated using National Semiconductor's advanced process. The parts of single chip as shown in **Fig. (4.2)** is described as follow[The National Semiconductor data sheet, 2005]:

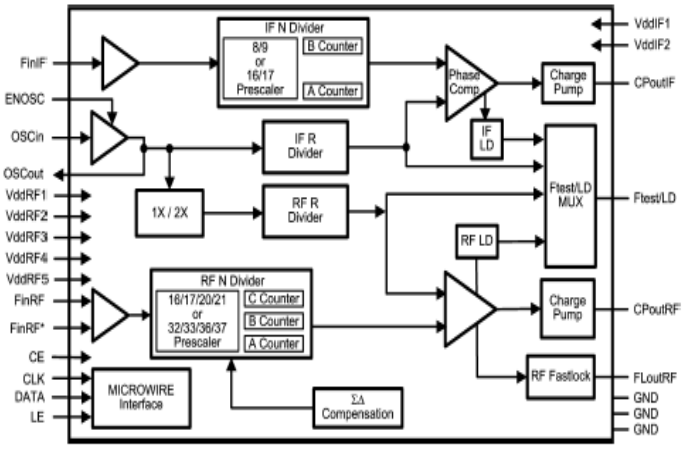

Fig. (4.2): Functional Block Diagram

- OSCILLATOR BUFFER, AND R COUNTER: The oscillator buffer must be driven single-ended by a signal source, such as a TCXO. The OSCout pin is included to provide a buffered output of this input signal and is active when the OSC_OUT bit is set to one. The ENOSC pin can be also pulled high to ensure that the OSCout pin is active, regardless of the status of the registers in the LMX2486. The R counter divides this TCXO frequency down to the comparison frequency.
- PHASE frequency DETECTOR: The maximum phase detector frequency for the LMX2486 RF PLL is 50 MHz. However, this is not possible in all circumstances due to illegal divide ratios of the N counter. The crystal reference frequency also limits the phase detector frequency, although the doubler helps with this limitation. There are trade-offs in choosing the phase detector frequency. If this frequency is run higher, then phase noise will be lower, but lock time may be increased due to cycle slipping and the capacitors in the loop filter may become rather large.
- CHARGE PUMP: For the majority of the time, the charge pump output is high impedance, and the only current through this pin is the TRI-STATE leakage. However, it does put out fast correction pulses that have a width that is proportional to the phase error presented at the phase detector. The charge pump converts the phase error presented at the phase detector into a correction current. The magnitude of this current is theoretically constant, but the duty cycle is proportional to the phase error. For the RF PLL this current is programmable in 16 steps. Also, the RF PLL allows for a higher charge pump current to be used when the PLL is locking in order to reduce the lock time.
- N COUNTERS & ΣΔ modulator: The N counter divides the VCO frequency down to the comparison frequency. The RF N counter contains an 16/17/20/21 and a 32/33/36/37 prescaler. The LMX2486 delta-sigma modulator is programmable up to fourth order, which allows to select the optimum modulator order to fit the phase noise, spur, and lock time requirements of the system. In our system fractional modulus is 15000.

Voltage controlled oscillator

The voltage controlled oscillator (VCO) is selected to achieve the frequency range(2350-2750)MHz with minimum phase noise. LMX2531LQ2570E I.C. is used to cover the required frequency range[8]. LMX2531LQ2570E has the following specifications:

- Frequency range: (2336 – 2790) MHz.
- Output power : (-1dBm - 4dBm).
- Fine tuning sensitivity (Kvtune): (10 - 23)MHz/V.
- Output impedance: 50Ω.

Loop filter

In cases where the VCO requires a higher tuning voltage than the charge pump can operate, active filters are necessary. VCOs with high voltage tuning requirements are most common in broadband tuning applications.

The loop filter impedance is defined as the voltage output at VCO to the current injected at the charge pump in the single chip synthesizer. The expression of loop filter impedance Z(s) & the corresponding poles & zeros are shown below at various filter orders is shown below[Dean banerjee, 2005]

$$Z(s) = \{1 + sT_2\}/\{s(A_3 s^3 + A_2 s^2 + A_1 s + A_0)\} \text{ , where } T_2 = R_2C_2 \qquad \text{eq(4.1)}$$

A_3, A_2, A_1 & A_0 are the coefficients of filter. For our system, the order of filter is three. Therefore $A_4 = 0$ & the values of the rest of coefficients as follows:

$A_0 = C1 + C2$, $A_1 = C1C2R2 + (C1+C2)C3\ R3$ & $A_2 = C1\ C2\ C3\ R2\ R3$

For our design, the values of components of Filter as follow:

C1 = 1pF, C2= 4.7pF, C3 = 1nF, R2 = 220kΩ & R3 = 10Ω.

Loop B.W. = 400 KHz, damping factor = 0.8.
The opamp in this filter must be a low phase noise, therefore we select LM6211. this op amp is fabricated by national semiconductor with following specifications:

- ❖ Input bias voltage : 2.75 volt.
- ❖ Opamp negative supply: 0 volt.
- ❖ Phase noise c/c of opamp in our system is shown in **Fig. (4.3)**.

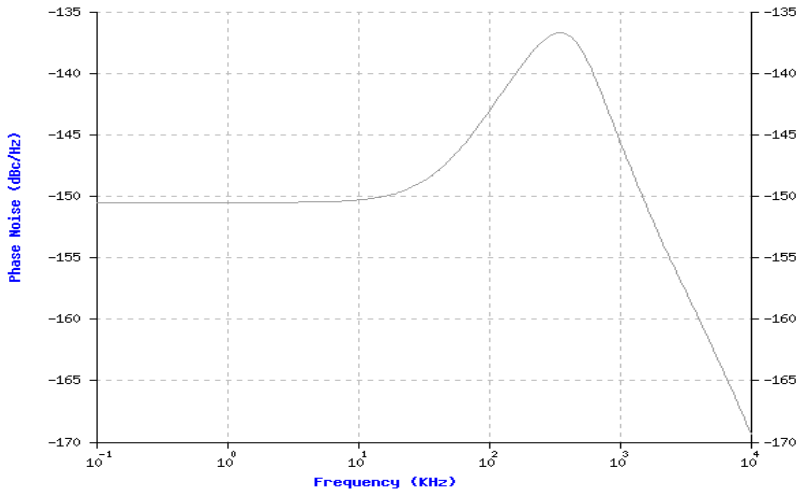

Fig. (4.3): phase noise c/c of op amp

frequency oscillator

The frequency of crystal oscillator (TCXO)in this system is 15 MHz , therefore the R counter is set to 3 to obtain 5 MHz. The phase noise c/c of TCXO in our system is shown in **Fig. (4.4).** From **Fig. (4.4) ,** it is clear that the TCXO is a low phase noise.

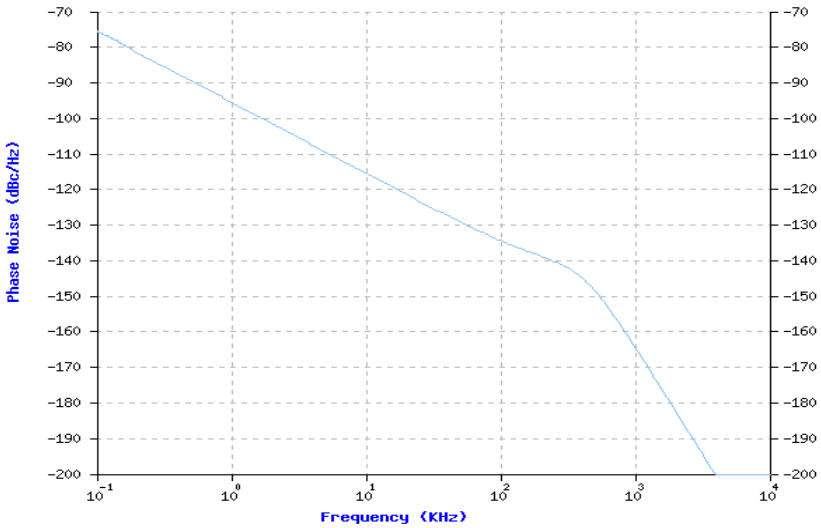

Fig. (4.4): phase noise c/c of TCXO

RESULTS

The system is simulated by software (WEBENCH) from National semiconductor company. The performance of frequency synthesizer consists of :

- Lock time: it is defined as the time needed for switching the synthesizer from one frequency to another . The lock time of our synthesizer is 8.9µsec for frequency switching (2350 - 2750)MHz as shown in **Fig. (5.1).**

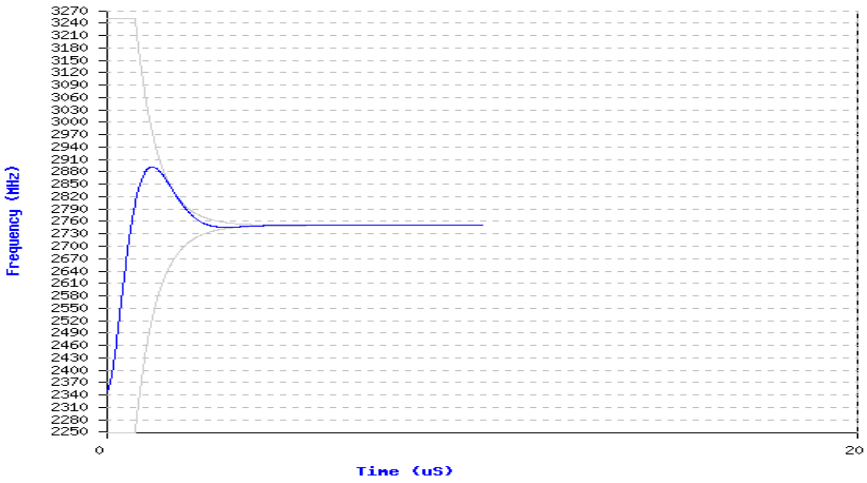

Fig. (5.1): lock time c/c of system

- Phase noise: it is the most critical parameters which describes short term frequency instability include fluctuations in signal's phase or frequency that less than 1sec. **Fig. (5.2)** shows the phase noise c/c of the system & VCO.

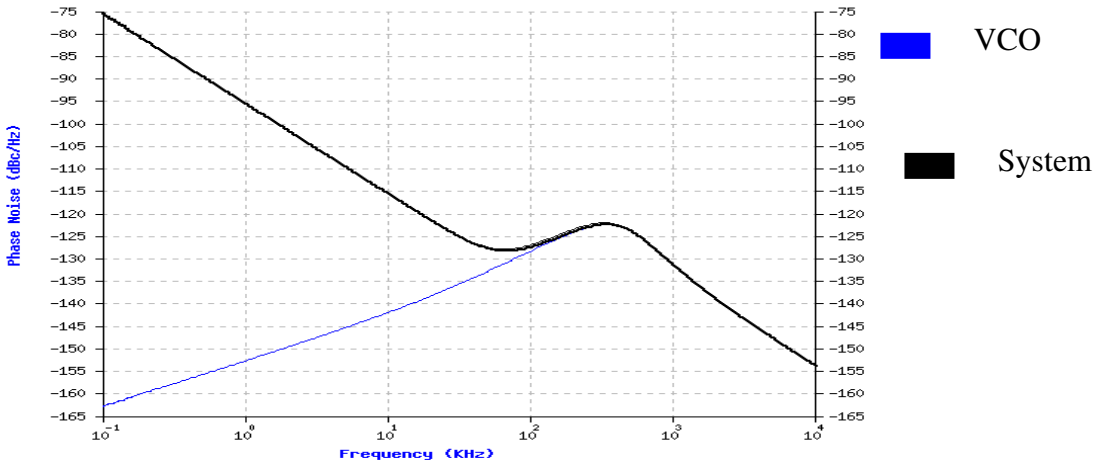

Fig. (5.2): phase noise c/c of TCXO

- Spurious output: denotes any unwanted products present at output of frequency synthesizer. The spurious level in this system is -69dB.

DISCUSSION & CONCLUSIONS

The implemented fractional N synthesizer has been presented with the basics of fractional PLL , including advantages & disadvantages. The implemented synthesizer achieve the requirements in section (4)with the following specifications:

- Frequency range : 2350 MHz – 2750 MHz
- Step size : 1kHz

- Switching speed : 8.9 μsec
- Phase noise : -115dbc/Hz @ 10 kHz
- Spurious : -69 dB

Among various techniques, the F-N technology has been selected since it has several advantages:

- Low feedback –divider ratio results in lower phase noise with fine step size.
- Low phase noise contributions are lowered by 20log(L),where L is the fractional modulus.
- Channel spacing is 1/L times smaller than an integer PLL.
- Larger loop B.W. results in lower lock time.

The development in I.C. technology provide the simplicity in the design of frequency synthesizer because it implements the PFD , prescalar, delta-sigma modulator & reference divider in single chip. this single chip has the following properties :

- Low power consumption.
- flexibility in selecting crystal oscillator frequencies.
- High reliability.

There is Direct digital synthesis (DDS) can be used to implement this system but it has drawbacks , its main disadvantage include the fundamentals limit of B.W. (maximum frequency o/p is less than one half the clock rate). Expanded B.W. requires higher clock rates , & therefore faster logic and more critical manufacturing & testing processes. There is Hybrid technique (DDS as reference oscillator) can be used to implement this system successfully but it has high cost relative to implemented system. Multi Loop PLL can satisfy this frequency range but these loops with their mixers increase spurious o/p signals , power dissipation , cost , size & complexity.

Table (6.1) shows a fair comparison with another work in 2003 includes design of an integrated CMOS PLL frequency synthesizer consists of two loops.

Table(6.1) comparison between implemented system with multi loop system

System parameters	Frequency range(GHz)	Step size	Switching time	Phase noise	Spurious level	Number of loops
Multi loop implemented In 2003	2.4 – 2.5	1MHz	30 μs	-83 dB/Hz @10 KHz	-60 dBc	2
System implemented.	2.35 – 2.75	1kHz	8.9 μs	-115dB/Hz @10 KHz	-69dBc	1

Table (6.2) shows a fair comparison with another work in 2004 includes design of a fully integrated Fractional-N frequency synthesizer for wireless communications.

Table(6.2) comparison between implemented system with a fully integrated Fractional-N frequency synthesizer

System parameters	Frequency range(GHz)	Step size	Switching time	Phase noise	Spurious level	Number of loops
Fractional-N implemented In 2004	2.4 – 2.4853	10kHz	10 μs	-90dB/Hz @10 KHz	-48 dBc	1
System implemented.	2.35 – 2.75	1kHz	8.9 μs	-115dB/Hz @10 KHz	-69dBc	1

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