

## ECG SLANTLET TRANSFORM WITH FPGA DESIGN

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### ABSTRACT

The ECG is used for the clinical analysis of physiological data has occurred in the field of cardiology. Certain abnormalities of the ECG are quite well defined and can be readily identified. The digital signal processing Slantlet Transform is used in the feature extraction of ECG monitoring and Diagnosis system to convert the continuous ECG signal to a form can be classified by a classifier of the ECG monitoring and Diagnosis system to detect the cardiac abnormalities.

In this paper, FPGA is used to build the slantlet Transform of the ECG feature extraction .VHDL program of FPGA is used in the work, the obtained output results are similar to the past work results, which is built by using Mat Lab program, in accuracy and closing to the original ECG signal. Using FPGA decreases the cost and time for building hardware system of ECG Monitoring and Diagnosis system. It also gives more flexibility than the alternate approaches. Mat-Lab program is used only for displaying the input and output discrete signals of slantlet transform.

### الخلاصة:

يستعمل تخطيط القلب الكهربائي لغرض التحليل الطبي للبيانات الفسلجية التي تحدث للقلب. الحالات غير الطبيعية المؤكدة للتخطيط الكهربائي للقلب هي معرفة بشكل واضح ويمكن تحديدها. إن التحويل (Slantlet) في معالج الإشارة الرقمية يستعمل في نظام المعاينة والتشخيص لتخطيط القلب الكهربائي لاستخراج خاصية إشارة تخطيط القلب الكهربائية المستمرة حتى يمكن تصنيفها بواسطة نظام تصنيف في نظام المعاينة والتشخيص لتخطيط القلب الكهربائي لاكتشاف الحالات غير الطبيعية للقلب.

تم استعمال المبرمج الحقلي لمصفوفات البوابة (FPGAs) في هذا البحث لبناء التحويل (Slantlet) لاستخراج خاصية تخطيط القلب الكهربائي. تم استعمال برنامج (VHDL) التابع ل (FPGAs) في هذا العمل كانت النتائج مقارنة لنتائج عمل سابق تم بناءه باستخدام برنامج (Mat-Lab) من ناحية الدقة والمقاربة مع

الإشارة الأصلية، لكن استعمال (FPGAs) قلل الوقت والكلفة اللازمين لبناء الدائرة الالكترونية لنظام المعاينة والتشخيص لتخطيط القلب الكهربائي كما انه يعطي مرونة أكثر من أي نظام بديل آخر. وقد تم استخدام برنامج Mat-Lab فقط لعرض الإشارات الداخلة إلى التحويل Slantlet والخارجة منه.

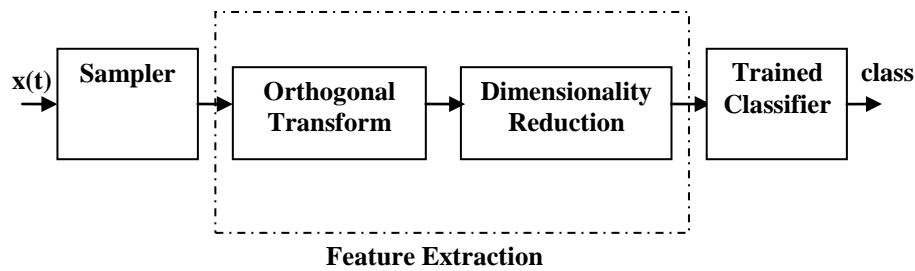
## INTRODUCTION:

The human heart is a complex muscular pump. Owing to the importance of the heart, a great interest has been given to monitor the heart operation, to detect its abnormalities. ECG measurements are used to monitor the contraction of the cardiac muscles by measuring the propagation of electrical depolarization and repolarization in the atria and ventricles. The ECG interpretation is important for cardiologists to decide diagnostic categories of cardiac problems.

The ECG pattern recognition as shown in fig. 1 is studied and programmed by Mrs. Rasha Thabit in her thesis . The first block is the sampler, where is necessary to convert the continuous ECG electrical signal ( $x(t)$ ) to a discrete one. The recognition of cardiac abnormalities is done in the third block by using neural network, depending on the features representing the ECG signal. Different types of digital signal processing transformation are tested in feature extraction block of ECG pattern such as FFT, Discrete Wavelet Transform and SLT, etc. In the thesis of Rasha, SLT gave better results than the other systems because it is the more accurate system, where the results of classification in the third block (neural network) has minimum percentage error rate, when SLT is used with respect to other types. Mat Lab program is used to implement the thesis work.

In this paper, FPGAs is used to build the SLT of ECG feature extraction instead of using Mat Lab program, to design a hardware circuit for this part..

FPGA is on the verge of revolutionizing digital signal processing. Many front-end digital signal processing algorithms are now most often replaced by FPGAs. This allows users to by pass the hardware design engineer leading to a significant reduction in development time and cost. VHDL program is used to build FPGA SLT design, where it is widely used in this field to offer software implementation. Different types of ECG signals are used to test the new system, by applying the samples of these signals to the ECG feature extraction block, which is built by FPGA. The input and output signals of the feature extraction block are plotted using Mat Lab program.



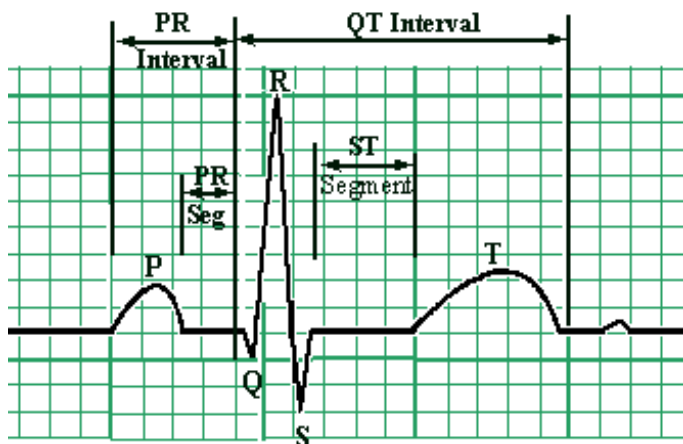
**Fig. 1: Pattern recognition system**

### DESCRIPTION OF THE ECG WAVEFORM:

Atypical ECG waveform is shown in fig. 2. The initial wave is the P-wave, it is small and rounded. Next a sharp combination wave known as QRS complex which is comprised of the sharp downward Q-wave, followed by the upward R-wave and subsequently the downward S-wave. The final wave, T-wave is rounded. The R-R interval represents the period from the R-peak of one beat of the ECG signal to the next R-peak. The P-R interval represents the period from the start of the P-wave to the beginning of the QRS complex, Q-T interval represents the period from the beginning of the QRS complex to the end of T-wave.

There are 12-lead ECG system, which includes three limb leads (I, II or (MLII), III), three augmented leads (aVR, aVL, aVF) and six precordial leads (V1, V2, V3, V4, V5, V6). It is the commonly used ECG system in clinic or health care centers.

Abnormalities of cardiac rhythm are easy to work out, by looking at the shape and width of the ECG waveforms such as P-wave, Q-wave, ST segment and T-wave. Then, the heart disease is diagnosed depending on the ECG waveform shape, such as Right Bundle Branch Block, Left Bundle Branch Block, Myocardial Infarction, Ventricular Tachycardia and Fibrillation.



**Fig. 2: Typical ECG waveform**

### Feature Extraction Using Slantlet Transform:

The slantlet filter bank used in feature extraction is based on three-scale filter bank as shown in fig. 3. The L-scale filter bank has  $2L$  channel. The low pass filter is to be called  $h_L(n)$ . The filter adjacent to the low pass channel is to be called  $f_L(n)$ . Both  $h_L(n)$  and  $f_L(n)$  are being followed by downsampling by  $2^L$ . The remaining  $2L-2$  channels are filtered by  $g_i(n)$  and its shifted time reverses for  $i = 1, \dots, L-1$ . Each is to be followed by downsampling by  $2^{i+1}$ . Note that in the slantlet filter bank, each filter  $g_i(n)$  appears together with its reverse, while  $h_i(n)$  does not appear with its time reverse. It always appears paired with the filter  $f_i(n)$ . The filters  $g_i(n)$ ,  $h_i(n)$  and  $f_i(n)$  have two zero moments that is, their inner products with linear polynomial sequences are zero.

The sought-after filter  $g_i(n)$  is to be linear over the interval  $n \in \{0, \dots, 2^i - 1\}$  and over the interval  $n \in \{2^i, \dots, 2^{i+1} - 1\}$ , therefore, it is described by four parameters and can be written as:

$$g_i(n) = \begin{cases} a_{00} + a_{01}n & \text{for } n = 0, \dots, 2^i - 1 \\ a_{10} + a_{11}(n - 2^i) & \text{for } n = 2^i, \dots, 2^{i+1} - 1 \end{cases} \quad (1)$$

Where

$$\begin{aligned} m &= 2^i \\ s_1 &= 6\sqrt{m/((m^2 - 1)(4m^2 - 1))} \\ t_1 &= 2\sqrt{3/(m \cdot (m^2 - 1))} \\ s_0 &= -s_1 \cdot (m-1)/2 \\ t_0 &= ((m+1) \cdot s_1/3 - m t_1)(m-1)/(2m) \\ a_{00} &= (s_0 + t_0)/2 \\ a_{10} &= (s_0 - t_0)/2 \\ a_{01} &= (s_1 + t_1)/2 \\ a_{11} &= (s_1 - t_1)/2 \end{aligned}$$

The same approach works for  $h_i(n)$  and  $f_i(n)$ , they can be written in terms of eight unknown parameters  $b_{00}$ ,  $b_{01}$ ,  $b_{10}$ ,  $b_{11}$ ,  $c_{00}$ ,  $c_{01}$ ,  $c_{10}$  and  $c_{11}$ .

$$h_i(n) = \begin{cases} b_{00} + b_{01}n & \text{for } n = 0, \dots, 2^i - 1 \\ b_{10} + b_{11}(n - 2^i) & \text{for } n = 2^i, \dots, 2^{i+1} - 1 \end{cases} \quad (2)$$



$$f_i(n) = \begin{cases} c_{00} + c_{01}n & \text{for } n = 0, \dots, 2^i - 1 \\ c_{10} + c_{11}(n - 2^i) & \text{for } n = 2^i, \dots, 2^{i+1} - 1 \end{cases} \quad (3)$$

Where

$$m = 2^i$$

$$u = 1/\sqrt{m}$$

$$v = \sqrt{(2m^2 + 1)/3}$$

$$b_{00} = u \cdot (v+1) / (2m)$$

$$b_{10} = u - b_{00}$$

$$b_{01} = u/m$$

$$b_{11} = -b_{01}$$

$$q = \sqrt{3/(m \cdot (m^2 - 1))} / m$$

$$c_{01} = q \cdot (v - m)$$

$$c_{11} = -q \cdot (v + m)$$

$$c_{10} = c_{11} \cdot (v + 1 - 2m) / 2$$

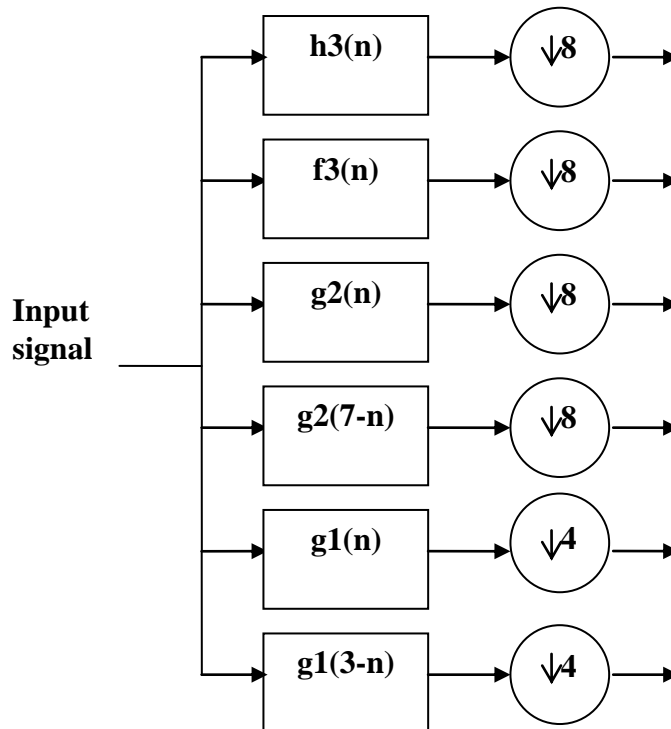
$$c_{00} = c_{01} \cdot (v + 1) / 2$$

The filters are implemented by a sequence of convolutions and down sampling, only four terms are needed to compute  $y_i(n)$ . The output sample of channel  $i$  is written as an inner product.

$$y_i(n) = \sum_{k=0}^{2^{i+1}-1} x(2^{i+1}n + k) \cdot g_i(k) \quad (4)$$

$$y_i(n) = a_{00} \sum_{k=0}^{2^i-1} x(2^{i+1}n + k) + a_{01} \sum_{k=0}^{2^i-1} kx(2^{i+1}n + k) + a_{10} \sum_{k=0}^{2^i-1} x(2^{i+1}n + (k + 2^i)) + a_{11} \sum_{k=0}^{2^i-1} kx(2^{i+1}n + (k + 2^i)) \quad (5)$$

The same equation will be used for  $h_i(n)$  and  $f_i(n)$ , the number of  $x$  input data sampling for this work is 256 samples and the number of  $y$  output data sampling is dependent on the value of downsampling, which is limited by the value of  $L$  and  $i$ .



**Fig. 3: 3-scale slantlet filter bank**

#### **FPGA DESIGN OF SLANTLET TRANSFORM:**

VHDL program provides language constructs for parametrizing and customizing designs, and for definition and usage of design libraries. These constructs enable a designer to generate a functional design independent of the specific technology and customize this generic design at a later stage. Specifically, library, use clause, package, and configuration declarations of VHDL are used for grouping or categorizing various components into design libraries and for customizing designs to use components in these libraries.

Several levels of components are nesting in the design of SLT. Fig. 4 shows the composition aspect for a configuration declaration of wiring and testing the SLT components architecture (architecture is a statement in VHDL program), where Slantlet Transform level (top level) and SLT filters level (second level) are shown in the figure. The Slantlet Transform level is the block of the whole SLT architecture. Inside this top level, SLT filters blocks are used as another level (filters level), each filter has a specified architecture.

Algorithm for the Slantlet Transform level (SLT block) is:

Step 1: Read a Text file of sampling data of ECG waveform (input data file), which is taken from MIT-BIH ECG database. A specified procedure (procedure is a

- VHDL statement) is used to read only 256 sampling values (real values), where the ECG waveform is repeated after that .
- Step 2: Convert these real values to binary values, with eighteen bits. A specified procedure is used for this operation. The binary values are stored in XX matrix.
  - Step 3: Give the XX matrix to the second block (filter block), the six filter blocks receives the XX matrix in parallel.
  - Step 4: SLT block receives the output of filters by a matrix Y with 32 cells for h3, f3 and g2 filters output and 64 cells for g1 filter output, depending on the downsampling of each filter. Each cell with thirty six bits length.
  - Step 5: The binary values of Y matrix are converted to real values by a specified procedure.
  - Step 6: write the real values in a text file (output data file) by a procedure.

Algorithm for the filters level (filter block) is:

- Step 1: Take the XX matrix from the SLT block.
- Step 2: Apply eq. (5) by replacing XX in x matrix and replacing filters functions g, h and f with their equations (1,2 and 3) respectively in eq. (4). Y output is obtained as a result. Specified circuit design is used to apply eq. (5), as shown in fig. 5.
- Step 3: Return Y matrix to the SLT block.

Fig. 5 shows the block diagram of the filters architectures design in the second level. This design is applied for the filters with downsampling by eight such as h3, f3 and g2.

In the design eight values of inputs data x are taken at each time. The first four inputs data from the eight values are added by adder component, the component has four inputs each input eighteen bits and one output acts the result of addition. The first four inputs data are also multiplied by k as in eq. (5). Multiplier component is used to multiply the four inputs data with four k values to obtain four results of multiplication (parallel multiplication), each input and output of this multiplier are eighteen bits. Another adder component is used to add the four results of multiplier component. The same operation is done for the second four inputs data, also two adders and one multiplier are used for the second four inputs data.

Four multipliers are used to multiply the outputs of four adders with filter constants (a, b or c as in eq. (5)). Each multiplier has two inputs, each one is eighteen bits. One output result of multiplication thirty six bits. At last the four outputs of multipliers are added by adder component with four inputs, each input thirty six bits and one output result of addition thirty six bits.

The output is loaded in the matrix of output data Y. This operation is repeated for another eight values of input data. The same design is used for the g1 filter but four inputs data are taken at each time.

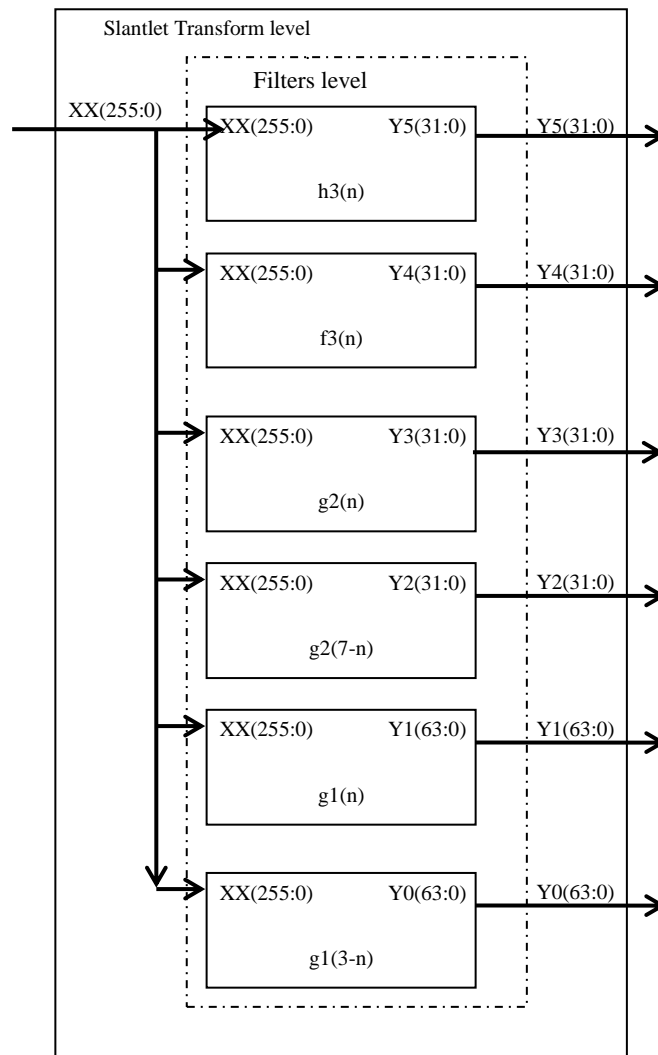
### **IMPLEMENTATION AND RESULTS:**

The whole FPGA design of SLT is implemented by VHDL program. The output of the low pass filter h3 (Y5) is the approximation of the signal and the other outputs are the details, therefore the output of the h3 filter is only displayed to obtain a close signal to the input one.

The input ECG signals are taken from MIT-BIH ECG database; the records 202,102 and 111 are used for Normal, Paced and Left Bundle Branch ECG signals respectively. 256 samples are enough to take from the sampling data file as input to the SLT filters, where the same data are repeated after that. The output of the h3 filter is 32 samples of data.

The input and output ECG samples real data, which is written in input data text file and output data text file are plotted using MAT-LAB program. The results are shown in fig. 6, fig. 7 and fig. 8 for normal, paced and left bundle branch ECG signals respectively. The continuous ECG signal for a patient is shown in (a), the ECG signal after the sampler (input to SLT) is shown in (b) and the signal after SLT is shown in (c), a single beat of MLII signal for normal and left bundle branch is taken and a single beat of V5 for paced beat is taken.





**Fig. 4 : Composition aspect of the Slantlet Transform for testing ECG feature extraction**

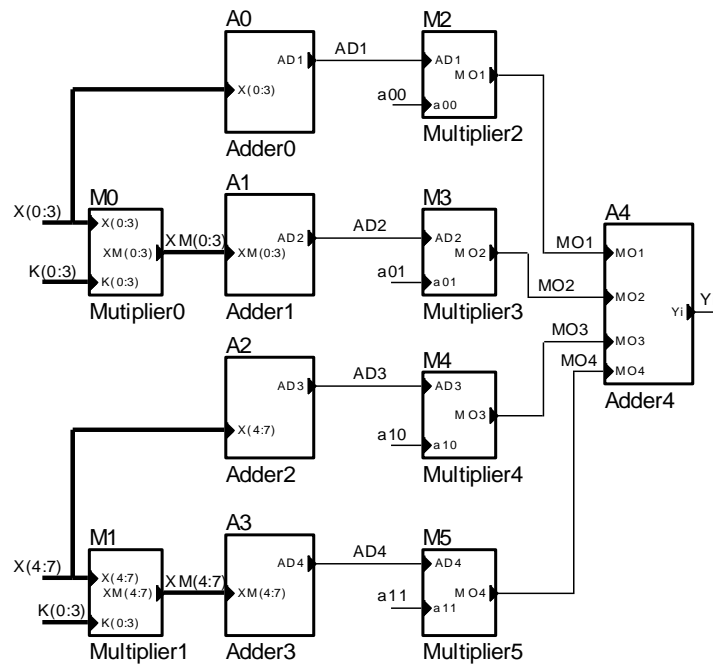
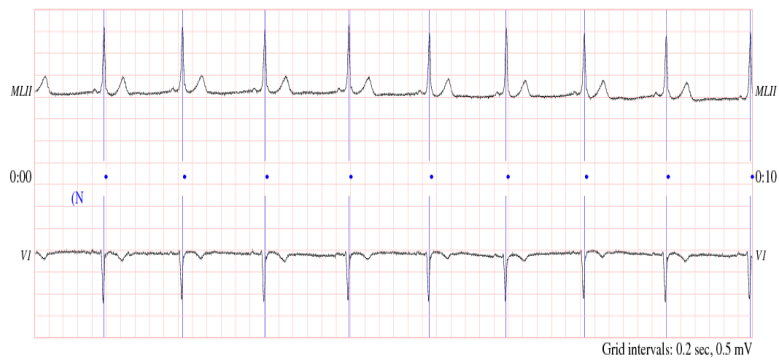


Fig. 5 : Block diagram of filter architecture design.

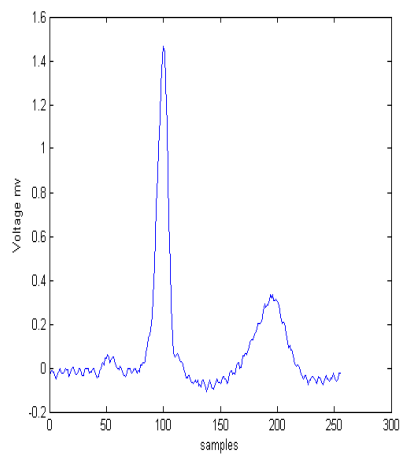
## CONCLUSIONS:

The work with VHDL program gives output waveform of SLT very close to input one. It is clear from the output signal figures, that is the output waveform has the features of the original ECG signal to accurately classify the heart arrhythmias.

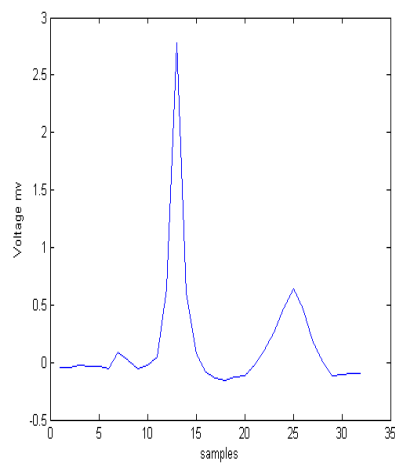
As in any high level language, VHDL allows the definition and usage of functions and procedures. In addition to the important hardware implications of subprograms, these language constructs greatly improve readability and organization of a hardware description.



(a)

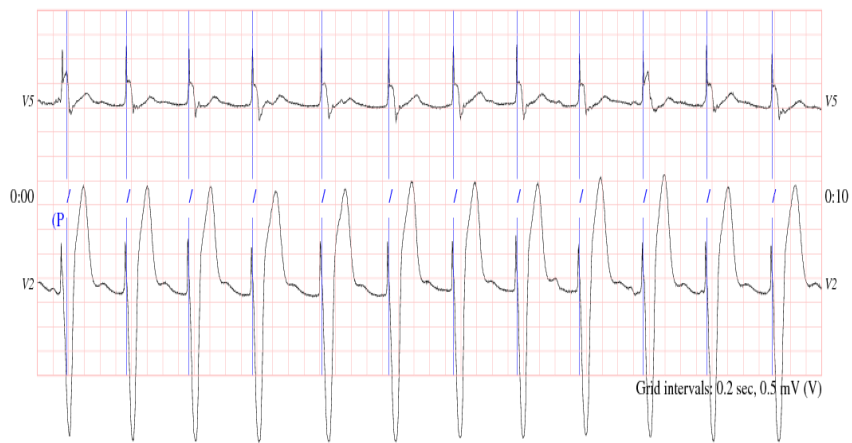


(b)

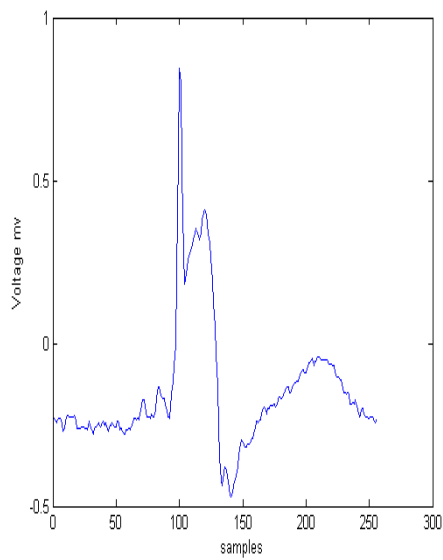


(c)

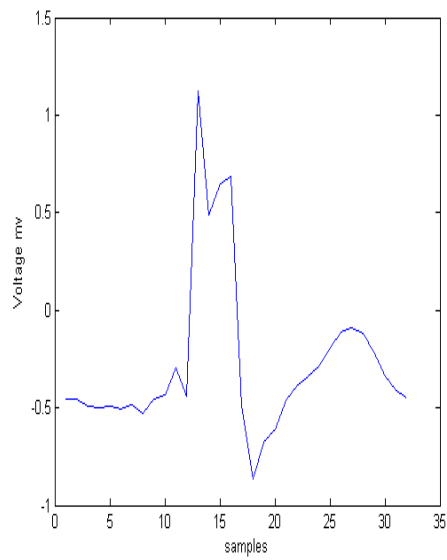
**Fig. 6:**  
**(a) The ECG record (Normal Sinus Rhythm).**  
**(b) The Extracted single beat.**  
**(c) 32 samples of the SLT (h3 output).**



(a)



(b)



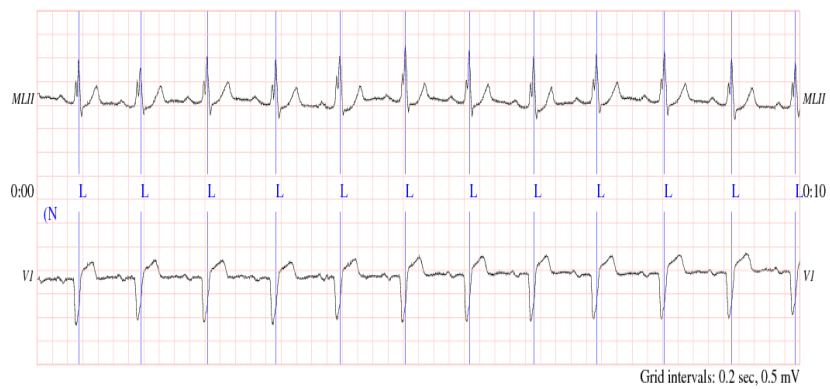
(c)

**Fig. 7:**

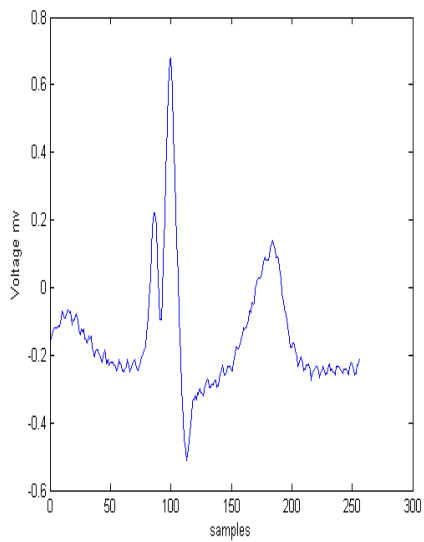
**(a) The ECG record (Myocardial Infarction (Paced beats)).**

**(b) The Extracted single beat.**

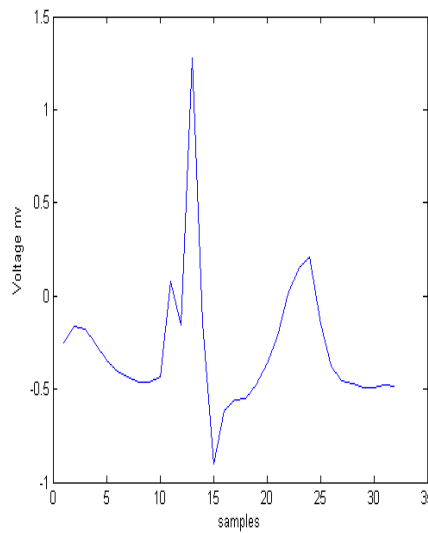
**(c) 32 samples of the SLT (h3 output).**



(a)



(b)



(c)

**Fig. 8:**  
**(a) The ECG record (Left Bundle Branch).**  
**(b) The Extracted single beat.**  
**(c) 32 samples of the SLT (h3 output).**

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**LIST OF ABBREVIATIONS:**

ECG : Electrocardiogram.

FFT : Fast Fourier Transform.

FPGAs : Field Programmable gate arrays.

SLT : Slantlet Transform.

VHSIC : Very High Speed Integrated Circuit.

VHDL : VHSIC Hardware Description Language.