Implementation of a Proposed Load-Shedding System Using Altera DE2 FPGA

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ABSTRACT

A load-shedding controller suitable for small to medium size loads is designed and implemented based on preprogrammed priorities and power consumption for individual loads. The main controller decides if a particular load can be switched ON or not according to the amount of available power generation, load consumption and loads priorities. When the maximum allowed power consumption is reached and the user want to deliver power to additional load, the controller will decide if this particular load should be denied receiving power if its priority is low. Otherwise, it can be granted to receive power if its priority is high and in this case lower priority loads are automatically switched OFF in order not to overload the power generation. The main idea of the proposed LS controller is to minimize the amount of the isolated load without overloading the power system. In this paper, three versions of load shedding controller were implemented using Altera DE2-115 FPGA; with number of loads equal 32, 64 and 128 for each controller.

Keywords: Power Systems, Load shedding, Overload, FPGA.

بناء منظومة مقترحة لعزل الاحمال باستعمال مصفوفة البوابات المنطقية القابلة لإعادة البرمجة

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الخلاصـــة

في هذا البحث تم تصميم مسيطر لعزل الاحمال يتناسب مع احمال صغيرة الى متوسطة الحجم ويكون اساس العمل على أولويات ومقدار استهلاك قدرة مُبرمجة مسبقا ولكل حمل. المسيطر الرئيس يتحكم بتشغيل او اطفاء اي من الاحمال حسب ما متوفر من قدرة متولدة واستهلاك الحمل واولوية عمله. عند طلب المستفيد بتشغيل حمل اضافي وكانت القدرة المستهلكة عند الحد الاقصى المسموح بها عندها يقوم المسيطر باتخاذ قرار بمنع تجهيز القدرة الى الحمل إذا كان الحمل ذو اولوية واطئة او السماح بتجهيز القدرة لذلك الحمل إذا كان الحمل ذو اولوية عالية وفي هذه الحالة يقوم المسيطر بإطفاء الاحمال ذات الاولوية الواطئة لكيلا يحدث تحميل زائد على قدرة التوليد. الفكرة الرئيسة من منظومة عزل الاحمال المقترحة هي تقليل مقدار الحمل المعزول مع تجنب التحميل الزائد لمنظومة القدرة. خلال. في هذا البحث تم بناء ثلاثة نماذج لمنظومة عزل الاحمال باستعمال مصفوفة البوابات المنطقية القابلة للبرمجة من نوع DE2 من شركة Altera، لعدد احمال يساوي 23 و 64 و128 لكل مسيطر.

كلمات مفتاحية: أنظمة القدرة، عزل الاحمال، التحميل الزائد، مصفوفة البوابات المنطقية القابلة للبرمجة.

1. INTRODUCTION

Load shedding is a procedure to disconnect parts of the load from the power system when the load demand exceeds the amount the power generation can deliver. Such situation occurs due to different conditions such as hours of peak demand, disturbances causing tripping of lines connecting power plants to the main grid and disturbances causing load islanding. **Fig. 1** explains the situation of islanding, where, the load is isolated from the main generation and left connected with the cogeneration, which can be a small diesel generation, solar panels, inverters or any other small-scale power source. In any of these conditions, the power system will have poor conditions where the voltage and frequency will drop significantly below nominal values that can lead to a total shutdown. This happens when the frequency continues to decrease until it goes below the 47.5 Hz which is the under frequency limit value for the generation protection, **Rudez and Mihalic, 2011**. To avoid this undesirable condition, power utility authorities resort to load shedding where controlled isolation of loads is implemented. The optimum load shedding procedure should make a balance between two requirements; the first is to maintain the operation of the power system by shedding load in a timely manner, in this way the drop of frequency below the 47.5 Hz limit is avoided. The second is that sometimes-conservative load shedding can shed more loads than it is actually required and this may leads to unnecessary blackouts, which is also undesirable. Therefore, the optimum load shedding is when the amount of the isolated load is as low as possible while maintaining the continuity of the power system.

2. OVERVIEW OF LOAD SHEDDING SCHEMES

There are different load shedding schemes, all share the same purpose that is, when the power system is faced with the condition where input generation power is less than the output-consumed power. The following is a brief review of the basic schemes used in load shedding.

2.1 Breaker Interlock Scheme

This is the simplest method to implement load shedding where some of the load breakers are interlocked by hardwiring with the main source beaker. When the main source breaker is tripped for some reasons, the interlocked breakers are directly tripped without any time delay. The advantage of this scheme is that it is simple and fast since there is no processing required. The disadvantage is that, the choice, amount of the interlocked loads is fixed by the hardwiring, and it is not easy to change. Also, there is only one stage for load shedding which makes the designer work on the worst case scenario and in many situations this will shed more loads than it is actually necessary, **Shokooh, et al., 2011**.

2.2 Under Frequency Scheme

Under Frequency load-shedding (UFLS) is the most common scheme used in load shedding. Its idea is such that, in situations when the available generation is overloaded either because of losing a part of the generation due to a disturbance or because of high load demand at peak hours, the frequency starts to decay and the under frequency load shedding scheme detect the condition of power system overload by measuring the frequency or its derivative. The schemes that rely on frequency value as a criteria for load shedding work on a multistage tripping of loads with each stage having a frequency value and a time delay settings. **Table 1** shows an example of settings of a two stage under frequency load shedding, **Rudez and Mihalic, 2011**.

According to these settings when the frequency goes below 49.5Hz but still above 49.0Hz (due to loss of part of the generation), the UFLS waits for 0.5s time delay and then trips the 100MW load. If the frequency stabilizes above the 49.0Hz, no more load shedding is required, but if the frequency continues to drop below the 49.0Hz limit, the UFLS waits for the 2.0s before it trips the 300MW load. The time delay in the conventional UFLS can lead to power system collapse due to situations when fast frequency deterioration that the time delays in the UFLS cause the load shedding to be made when it is too late. **Rudez and Mihalic, 2011,** proposed an under frequency

load shedding that relies on the second derivative of the frequency as a source of information to estimate future values of frequency (frequency forecast), and when the calculated forecast frequency goes below the 47.5Hz value the system starts shedding loads according to the value of the forecasted frequency. Performance analysis showed that this method could maintain the operation of the power system by shedding loads less than the conventional under frequency load shedding.

2.3 Under Voltage Scheme

The under voltage load shedding (UVLS) scheme relies on voltage measurement as a criterion instead of frequency to monitor the condition of the power system, the main difference between the two schemes is that frequency value is the same throughout the entire power system grid, so, different nodes in the power grid measure the same frequency value. While for the voltage, the situation is not the same, different nodes measure different values of voltage due to drops across transmission lines. In general, nodes closer to generation units measure higher values of voltage and nodes far from generation measure lower values of voltage. **Otomega, et al, 2007**, proposed an UVLS system where distributed controllers are used around the power system. Each controller monitors the transmission voltage and controls a group of loads. The decision of one controller is made by measuring the voltage V at the controller's node and comparing to a certain threshold V_{th}, if V goes below V_{th}, an amount ΔP of load is shed after a time T. The values of ΔP and T are dynamically determined according to the measured value of V. In this system, the choice of the load to be shed is better determined because the nodes with the lowest voltage are expected to shed loads more than the nodes that have higher values of voltage. since the load is expecting the power utility to deliver the voltage at its nominal value, it will make more sense when the power system isolate the load that it can't provide the proper voltage level to it.

2.4 Power Based Load Shedding

The power-based load shedding (PLS) works on gathered information about the amount of available generation and consumed power and it reacts when there is a detection of deficiency between the actually generated and the consumed power. In order to optimize the performance of this scheme (PLS), it only requires that the information gathering technique to be optimal in terms of accuracy about how much is the generated and consumed power as well as the time delay required to deliver this information to the LS system. Therefore, such systems are only useful for small to medium scale power systems like isolated industrial plants, oil fields, mines, etc. **Giroletti, et al, 2012**, proposed a hybrid LS system were power based scheme is combined with frequency based LS.

2.5 Controller Based Load Shedding

In Controller based load shedding (CLS), either a programmable logic controller (PLC) or a microcontroller is used as a main controller of LS. This is to make the LS system configurable to a specific small-scale application. This scheme can be considered as a simplified version of the PLS scheme where the difference between the available power and the consumed power is monitored and the load shedding is scheme is performed according to the calculated power shortage. It has the advantage of being fast and optimal in terms of amount load shedding. The proposed LS scheme of this work falls under this category and further details will be provided in the next section.

2.6 Intelligent Load Shedding Scheme

Intelligent load shedding (ILS) is different from the previously mentioned schemes in its concept where system has the capability of predicting the behavior of the power system in terms of frequency and voltage values in cases of contingencies that cause loss of generation, increase of load demand or any change in the power system configuration. The capability of predicting the

behavior of the power system necessitate several requirements to be provided for the ILS system, **Shokooh, et al., 2011**,

- The power system configuration should be defined to the ILS system as a knowledge base.
- The ILS system should acquire information in the form of self-training and automatic learning to update the system knowledge base due to system changes.
- The ILS system should have sufficient (but still limited) number of data collecting points to map the complex power system to a proper model.
- Making fast and reliable decision on priority load shedding based on actual loading of status of each breaker.

Intelligent load shedding scheme is complex system where load-shedding tables are built according to previous knowledge of the power system status during contingencies and these tables are constantly updated through the real-time monitoring and simulation of the power system. As a result, when the ILS detects a power shortage and thus a need for load shedding, it will be equipped with the necessary knowledge to be correctly decide the optimal load to be shed in terms of amount and location with minimum time delay. Works that are based on ILS philosophy can be found in **Shi and Liu, 2014; Novikov and Karatayev, 2015 and Tamilselvan and Jayabarathi 2015**.

3. THE PROPOSED SCHEME

In this work, a controller-based load shedding (CLS) system is suggested, designed and implemented for small to medium scale load size like a large building, hospital, industrial plant… etc. The general idea is that the controller compares the total sum of the consumed power P_s with maximum allowable power consumption P_{max}. Before going into details, it is worth mentioning that powers measured and calculated can be either active power or apparent power, the apparent power which is simply $S=IV$ gives more indication about the load current I, this is important since the overload protections are based on current measurements. However, it should be noted that the apparent power S is a vector (complex value) quantity and in order to calculate the total apparent power as the sum of individual loads apparent powers, the power factor $\cos\phi$ of each load should be considered. An alternative way would be to use measurement to find the total load current I to calculate $S=IV$ but this requires additional hardware for current measurement like a current transformer (CT) which would increase the cost of the system. Alternatively the active power $P=IV\cos\phi$ which is the real part of S can be used and the active power of the individual loads can be added directly. However, this choice does not give a direct indication about the total current because power factor is required in the calculations. Another alternative is to deal with load currents that is equivalent to the choice of the apparent power S because the voltage can be considered constant for all loads and hence becomes just a scale factor between current and apparent power. If the apparent power or the current quantity is adopted an approximation calculation approach can be used to avoid the need of the power factor which is adding the magnitude of the individual loads apparent power or current. This will give total sum greater than the actual sum, due to the triangle inequality **Eq. (1)**.

$$|S_1|+|S_2|\geq|S_1+S_2| \tag{1}$$

This is equivalent to assuming that all loads power factors are equal which is considered as a worst-case scenario and can be adopted when simplicity and cost reduction is required. It will be up to the designer to choose the appropriate scheme depending on the specific application and/or the customer requirement. In this work, quantities are summed as real numbers and referred to a load power that can be either active power or apparent power with the approximation of equal power factors.

Each load that should be controlled by the shedding rules is assigned two index values and these two values are stored in the main load-shedding controller as lookup tables. The first is the power index value which defines the amount of power the specific load consumes, the second is the priority index which defines how much the load is important and hence whether it should be isolated first (for low priority loads) or kept connected (for high priority loads) in case of power shortage. In this system, the user does not have direct control on the load; instead, the user can only give the command of switching ON or OFF to the LS controller. The LS controller continuously poles all the load ON/OFF switches as the system input and the controller will process this input and decides which of the individual ON inputs should pass to the output as ON value (logic 1), so that their respective loads are actually switched ON, and which load are switched OFF even if their respective input switches are actually ON. **Figure (3)** shows a typical block diagram for the system hardware. The inputs to LS controller can be classified to two types; software and hardware. The software type is the entries of the power index and priority lookup tables **PIT** and **PRT** that are entered to the controller as user defined input settings values. The hardware input is the $\mathbf{L_{IN}}$ vector that represents the load status according to the user request (which load is to be ON and which to be OFF).

There is one more important parameter of the system, which is the P_{max} value. This value is defined both by hardware and software. It is assumed that the source of power is not a single source, which is generally the case where multiple generations are synchronized and connected in parallel. Therefore, for each source of generation, the nominal generation power is defined in the vector **PG** to the LS controller as user input settings. These generation sources can be either a standalone generator or a transformer connected to the main grid. The status of each source is defined to the LS controller by the vector $\mathbf{G_{IN}}$ as hardware input, both vectors **PG** and $\mathbf{G_{IN}}$ have length of N_G, which is the number of generation sources. Therefore, when a generation source is connected to the system, the respective bit in the $\mathbf{G_{IN}}$ vector is set and when that generation source is lost, the respective bit is cleared. This bit can be connected directly to an auxiliary contact of the circuit breaker connecting the generation source to the system. According to the above, the value of P_{max} is given by Eq. (2).

$$P_{\max} = \sum_{n=1}^{N_G} \mathbf{G_{IN}}(n).\mathbf{PG}(n) \qquad (2)$$

The nth components of the power index table **PIT** are measure of the nth load power consumption. Since there is a wide range of values of the power for all loads the storage space for these values will unnecessarily be large, therefore, the power index **PIT**(n) defined as the integer value of the ratio of the nth load to the smallest load as given in Eq. (3)

$$\mathbf{PIT}(i) = \left\lceil \frac{\alpha P(n)}{\min\{P(n)\}} \right\rceil \quad n = 1,2...N_L \qquad (3)$$

Where ⌈ ⌉ equals the smallest integer greater than x and α is a factor depending on the maximum and minimum load powers to make the range of load power index suitable for the storage space allocated for each entry of the power index. For example if the maximum load power is 3kW (or kVA) and the smallest load power is 100W (or VA) and the memory allocation space for the power index is 8 bits then the maximum index would be 255 then α should be 255×100/3000=8.5. It is important to note that the minimum load power does not mean the absolute minimum power because there are loads with small powers, in domestic applications such loads can be chargers of battery-operated devices, economic lightings…etc. Such loads do not need to be under the control of load shedding. It is up to the user to determine the minimum load power that should be under the

control of the load-shedding controller because obviously the complexity of the system depends on the number of loads that the LS controller can handle.

The priority table **PRT** defines the importance of the load, upon which the LS controller will decide if the load should be isolated or not in case the power demand exceeds the available power. For a given load, the value of **PRT**(*n*) is not related to the respective power index value **PIT**(*n*) it is only related to the type of load, for example a refrigerating load may be considered a higher priority load than a water heating load although the water heating load has a higher power index than the refrigerating load. The priority values can be either all distinct or there can be multiple loads of equal priority according to the user choice.

The typical algorithm used for the load shedding is explained by the flowchart shown in Fig. (4). Assuming the number of loads equals to N_L, the inputs are read as a vector of logic values $\mathbf{L_{IN}}$. The input vector is passed to another vector of equal size that is called the status vector **ST**. After that, the controller starts to calculate the sum of the power indices of the loads that have logic 1 in the status vector **ST**.

$$P_s = \sum_{n=1}^{N_L} \mathbf{PIT}(n).\mathbf{ST}(n) \qquad (4)$$

The power index sum P_s will be compared to the maximum allowable power consumption P_{max} which is a value provided by the power system authority above which the power generation cannot supply and if the sum of power indices is less than the maximum available power ($P_s \leq P_{max}$), the status vector will be passed to the output vector $\mathbf{L_{out}}$ and all loads that the user required to switch on will be switched on by the LS controller. If the power consumption is more than this value ($P_s > P_{max}$), the load shedding is activated and the LS controller starts resetting the entry in the status vector **ST**(x) that correspond to the lowest priority loads and the value of P_s is updated according to eq. (2) and the process is repeated until ($P_s \leq P_{max}$). Mathematically, this can be describes be the equation

$$P_s = \sum_{\mathbf{PRT}(n) \leq K} \mathbf{PIT}(n).\mathbf{ST}(n) < P_{\max} \qquad (5)$$

Where K is the minimum priority allowed by the load condition such that

$$P_s = \sum_{\mathbf{PRT}(n) \leq K+1} \mathbf{PIT}(n).\mathbf{ST}(n) > P_{max} \qquad (6)$$

This is a typical algorithm whose flowchart is shown in a simplified form in Fig. (4). The algorithm although works just fine and is adopted in many LS applications but it is not adopted in this work, the reason is that it has a disadvantage where in some situations the amount of load shedding is not optimal!

Consider the situation where a load with high value of power index and a low priority and that the LS situation required switching OFF that particular load due to its low priority, this can leave a gap between P_s and P_{max} i.e. P_{max}-P_s is not minimized, because high power index load has been eliminated in order to keep $P_s < P_{max}$. While on the other hand there can be loads of lower priority and lower power indexes that can be switched ON while maintaining the condition $P_s < P_{max}$ which is the ultimate objective of the LS system. The cause of the pitfall of this algorithm is that the **ST** vector is initialized with the $\mathbf{L_{IN}}$ vector and the priority processing is carried out in down-up direction. An alternative approach would be to initialize the **ST** vector with all zeros vector and starting filling the **ST** vector according to the $\mathbf{L_{IN}}$ vector with the priority processing in the up-down direction. This approach is adopted in this work and its flowchart is shown in Fig. (5).

This flowchart shows two nested loops the outer loop is the priority index (p) loop and the inner loop is the load number (n) loop. The idea of this flowchart is that the controller starts processing

the highest priority loads first giving them the advantage of being switched ON before the low priority loads. In each iteration of the outer priority loop, i.e., for a particular value of p, the priority table is checked for the loads that have this particular value of priority. This is achieved by running the inner loop for all values of n to check the condition PRT(n)=p. The design allows multiple loads to have equal priorities or the user can have all loads with different priorities. When the condition PRT(n)=p is satisfied, the status vector **ST** is updated according to the flowchart shown in Fig. (6), where the input vector $\mathbf{L_{IN}}$ is checked if the user has requested the n^{th} load to be switched ON which is given by the condition $\mathbf{L_{IN}}(n)=1$. If not then nothing is done and the value of n is incremented, if so, then the controller checks if the respective load power is less than the difference of the maximum allowable power P_{max} and the updated value of the power sum P_s, which is given by the condition $PIT(n)<P_{max}-P_s$. If this condition is satisfied then the LS controller grants permission to the respective load to be switched ON by setting its respective bit in the power status vector **ST** to 1, i.e., $\mathbf{ST}(n)=1$ and the power sum is updated by $P_s=P_s+PIT(n)$.
A mathematical description of this algorithm is described by the equation

$$P_{max} - \sum_{n} \mathbf{ST}(n).\mathbf{PIT}(n) < \min_{\mathbf{ST}(n)=1} \{\mathbf{PIT}(n)\} \qquad (7)$$

Where summation is run over the values of n such that all values of **PIT** are considered starting from 1 (highest priority) to N_L (lowest priority) excluding the values of n that violates the condition of eq. (5) and the values of n where $\mathbf{ST}(n)=0$. This algorithm guarantees that $P_{max}-P_s$ is minimized.

4. SYSTEM IMPLEMENTATION

The proposed system of LS was implemented on FPGA platform. The Altera DE2-115 board shown in Fig. (7), was used to implement the proposed system. The board hosts, the Altera Cyclone IV 4CE115 FPGA device, which contains 114,480 logic elements (LE's). The main components of the implemented LS system are shown in block diagram of Fig. (8), Fig. (9) shows the result of project compilation.

The top-level entity of the implemented project is a schematic file type (as shown in Fig. (10)), but all other entities are (.hdl) file type. The written VHDL code compiled and transferred to create a symbol. The created symbols can be put on the top-level entity and route easily.
The input ports of the top-level entity are the user load input vector, $\mathbf{L_{IN}}$, the generator input vector, $\mathbf{G_{IN}}$, system clock, ***clk***, as well as the push buttons and slide switches for the user editing.
The output ports of the top-level entity are the loads output $\mathbf{L_{OUT}}$, the generator output vector, $\mathbf{G_{OUT}}$, and the data and control signals to derive LCD.
There are two main processes in the top-level entity; the first process is editing the power index and priority tables that saved in memory. This part also includes accessing the LCD embedded inside the DE2-115 board where the user's entered values are displayed before storing in the memory block that represents the look up tables of power index and priority. The second part of the code is the LS controller described earlier.
The LS controller is designed to control 32, 64 or 128 loads (i.e. N_L=32, 64 or 128), and it has been show earlier that the LS controller body is in the form of two nested loops of size N_L. Therefore, the total delay for a complete loop will be proportional to N_L^2. The total time that the LS controller needs to pole the users' inputs, makes decision and updates the outputs is about 0.1 second, which is small enough that the user cannot notice. Therefore, the clock frequency of the **clk** signal must be chosen to be 10.24 kHz or more to maintain 0.1-second criteria for a system that shed 32 load according to eq.(8). If the controller is designed to control more loads, the clock frequency should be increased in order maintain the acceptable time delay given by eq. (8).

$$f_{clk} = \frac{N_L^{\,2}}{\tau} \qquad (8)$$

Where f_{clk} is the controller clock frequency, τ is the acceptable controller time delay and N_L is the number of loads. **Table 2** summarize the required clock frequency to achieve 0.1-second criteria with different number of loads. So, the clock frequency would be about 655.36 kHz for 256 loads system which is considered moderate in today's technologies so there will be no major concerns regarding power consumption, heat dissipation, etc.

5. SYSTEM TESTING AND RESULTS VERIFICATION

A priority based load-shedding controller is implemented to deals with small to medium power systems applications. In the implemented design, the amount of load to be shed is minimal unlike the traditional controllers based load shedding systems. The system was implemented and tested on FPGA platform and timing analysis showed that the system delay time is quite manageable.
To verify the implemented system, different case studies are presented as follow:

- The controller will shed 32 loads.
- The power delivered from FIVE different generators each with 200 KVA. (Totally 1000 KVA)
- The priorities and power consumption of each load are initially assumed as in **Table 2**.

The controller will calculate total required current due to the switched ON loads. If the total required power is less than maximum available power then there is no need to enter load-shedding algorithm. If not, the load shedding algorithm start to check the status of loads depending their priority level.
The controller will shutting down or starting generators depending on the required power. Therefore, if the total required current less than 800 KVA, then one of the five generators will shut down, and so on.

Input switches panel are used as a user load input vector (L_{IN}) (Device 1 to device 32) will connected to DE2-115. To verify the output of the controller (32 loads output L_{OUT}) we need 32 LED, and if the load is switched ON by LS controller then the corresponding LED will shine.
Table 3 lists four different cases to test the LS controller, for simplicity, the devices rearranged according their priorities from higher to weaker priority.

In the first case, the sum of the required power (calculated by controller) are less than the maximum available power (i.e. 970 KVA < 1000 KVA delivered by 5 generators), so no load shedding needed.

In case 2, the required power (1070 KVA) is higher than the maximum available power (1000 KVA), so, the controller starts LS algorithm, the controller take a decision to turn Device (28) OFF, which has weaker priority between the turned ON devices. The consumed power after LS algorithm be 950 KVA.

The main advantage of the proposed LS controller is founded in case 2. The user need to switch devices (18 and 20) ON which has the lowest priorities between the turned ON devices (lower than D28 priority). As mentioned in the previous case, Device (28) and any other devices with lower priorities will turned OFF, so the rest power (not used) will be 50 KVA. The extra power required to derive D18 and D20 is 25 KVA so the controller will support them with power and the rest power (not used) will be 25 KVA and the total consumed power be 975 KVA.
The last case (i.e. case 5), the user need to switch device (26) ON as well as the other needed loads. The controller will shut down D28, D20 and D18, and the total required power will be 990 KVA, but the rest power (10 KVA) is enough to derive D18 only (which need 6 KVA) and the rest power become just (4 KVA) and total power consumed will be 996 KVA.

6. CONCLUSION

A priority based load-shedding controller is implemented suitable for small to medium power systems applications. In the suggested approach- as shown in **Table 3**- the amount of load to be shed is minimal unlike the traditional controller based load-shedding systems. The main difference is that the proposed LS system allow power to be delivered to a lower priority loads under the condition that the total power delivered is less than the maximum available power. The system was implemented and tested on FPGA platform. The hardware implementation produced small time-delay that is quite suitable for LS application.

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Figure 1. The situation when part of the load is islanded.

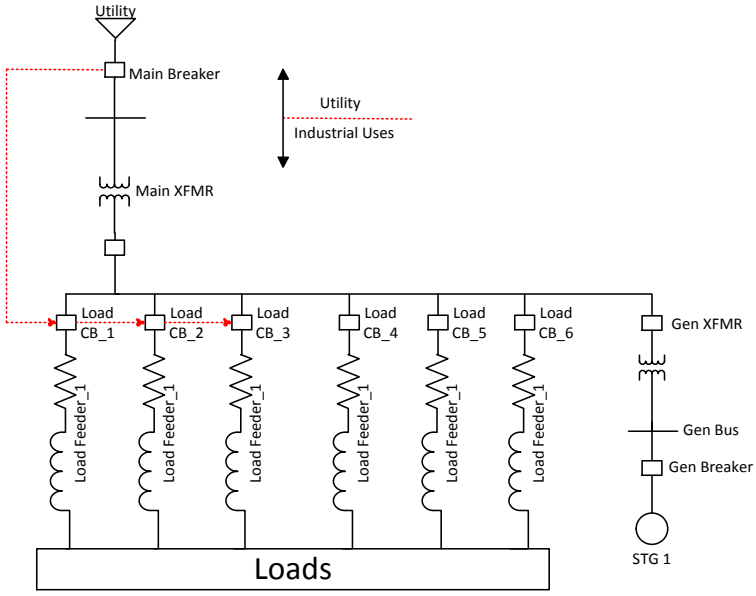

Figure 2. Breaker interlock scheme.

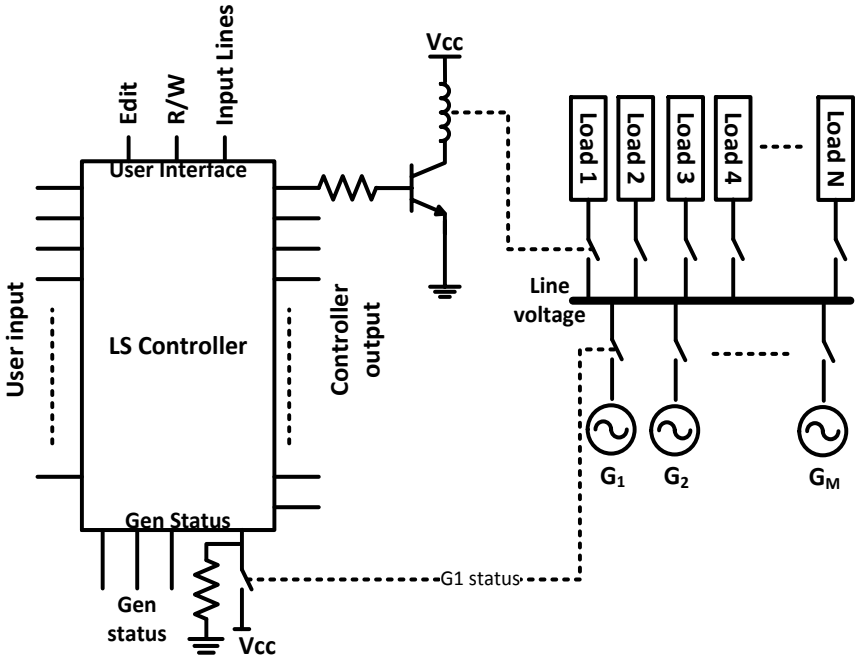

Figure 3. Block diagram of the proposed LS system.

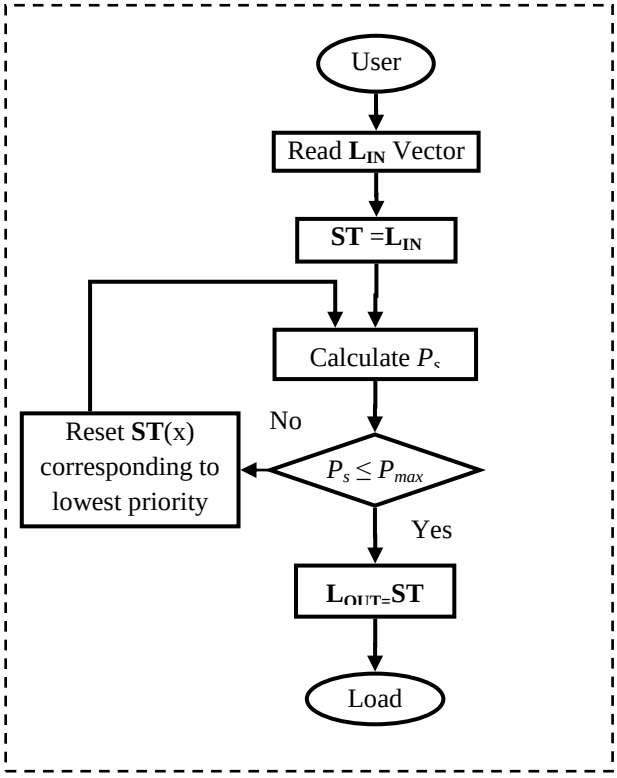

Figure 4. Flow diagram of a typical priority based LS.

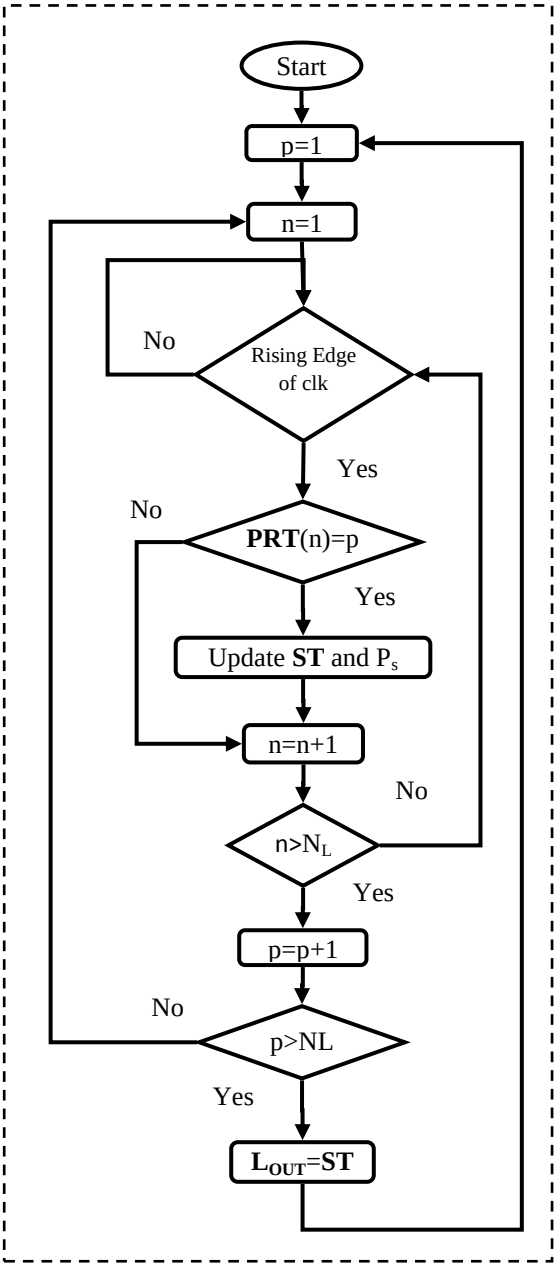

Figure 5. A flowchart of the implemented LS algorithm.

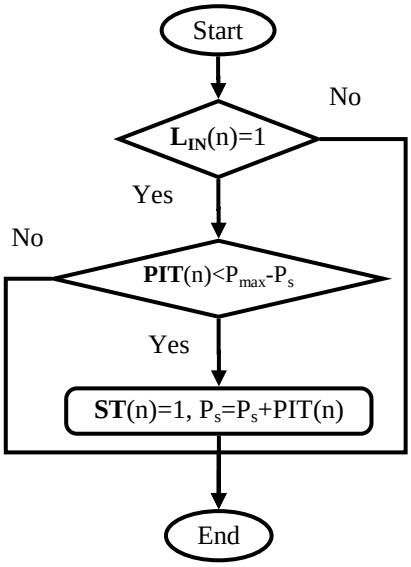

Figure 6. Details of updating ST and P_s.

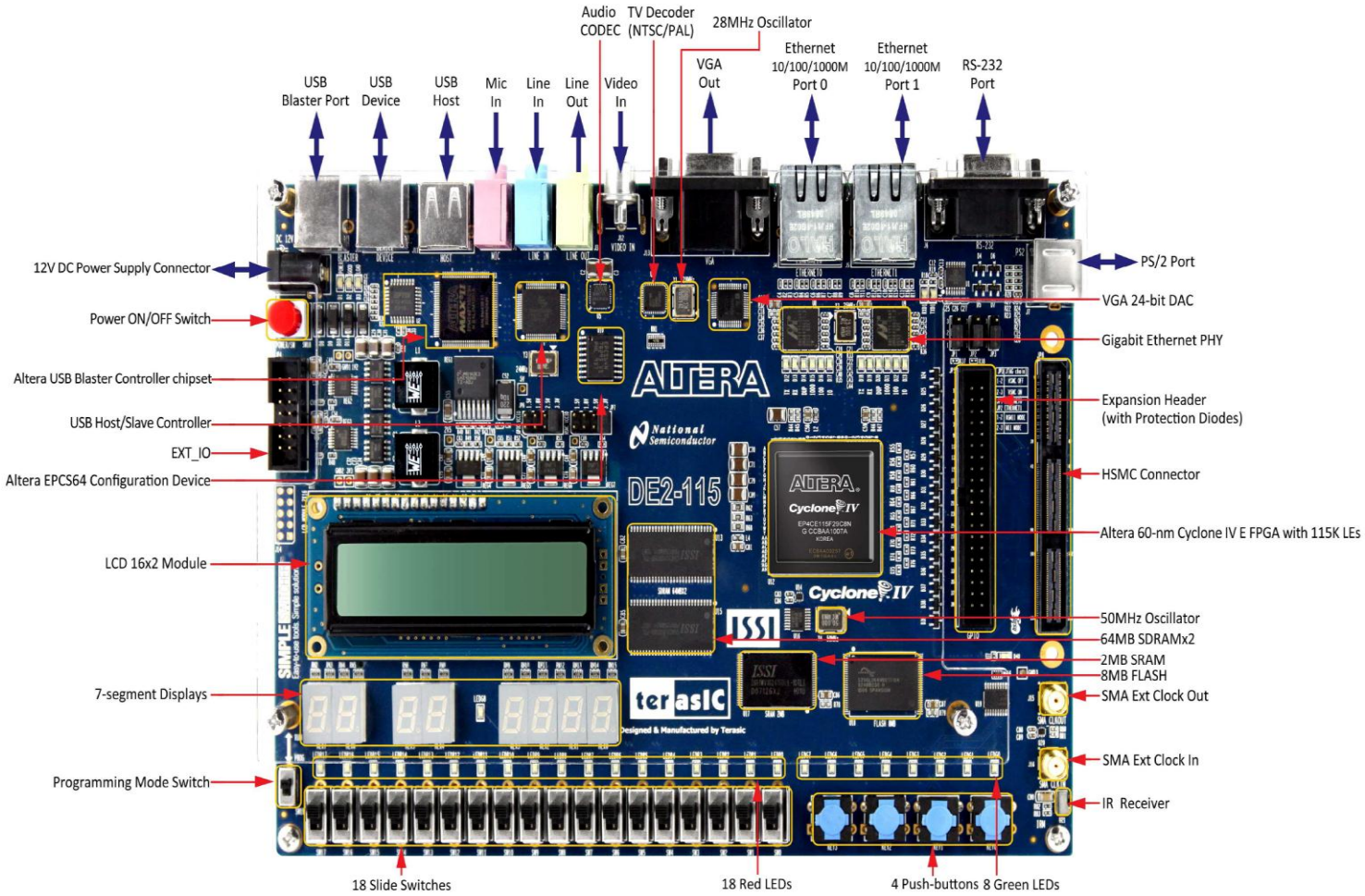

Figure 7. Altera DE2-115 FPGA (Top view).

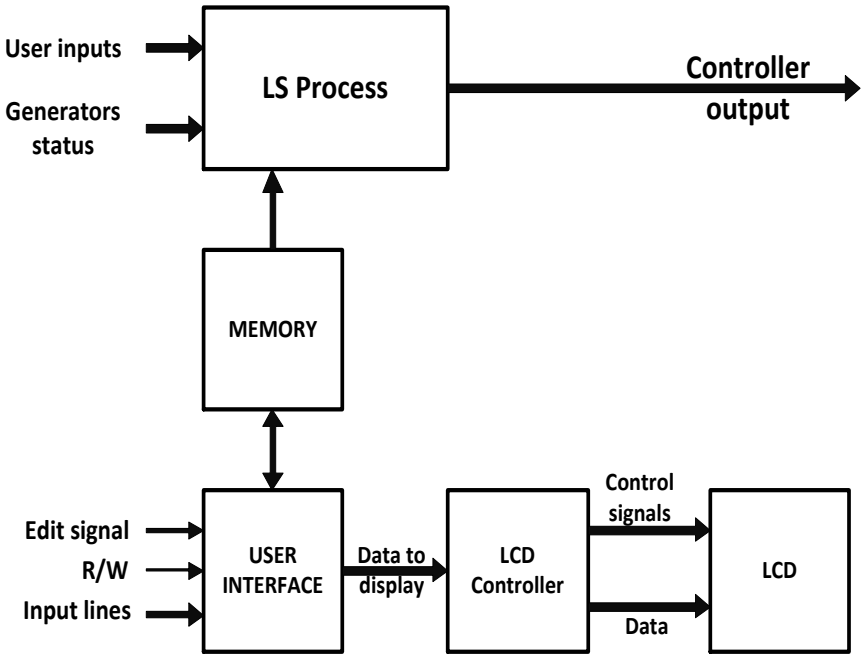

Figure 8. Block diagram showing the internal logic of the implemented LS system.

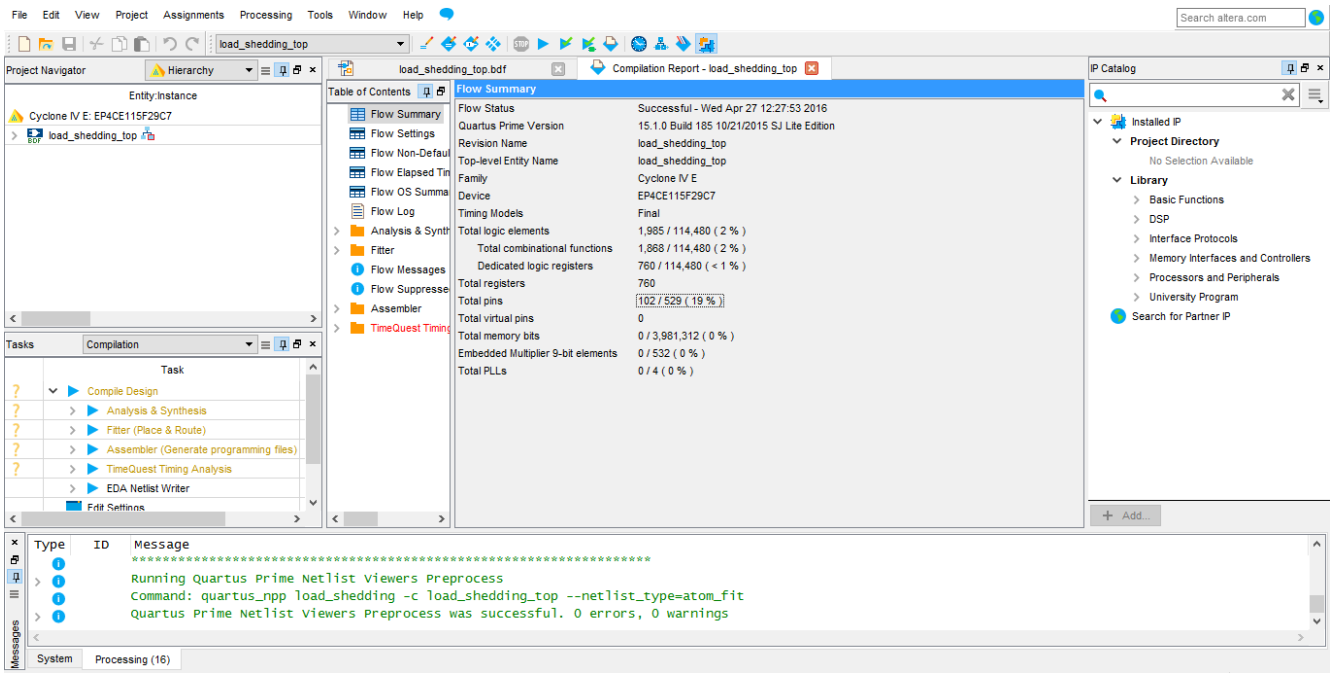

Figure 9. The result of project compilation.

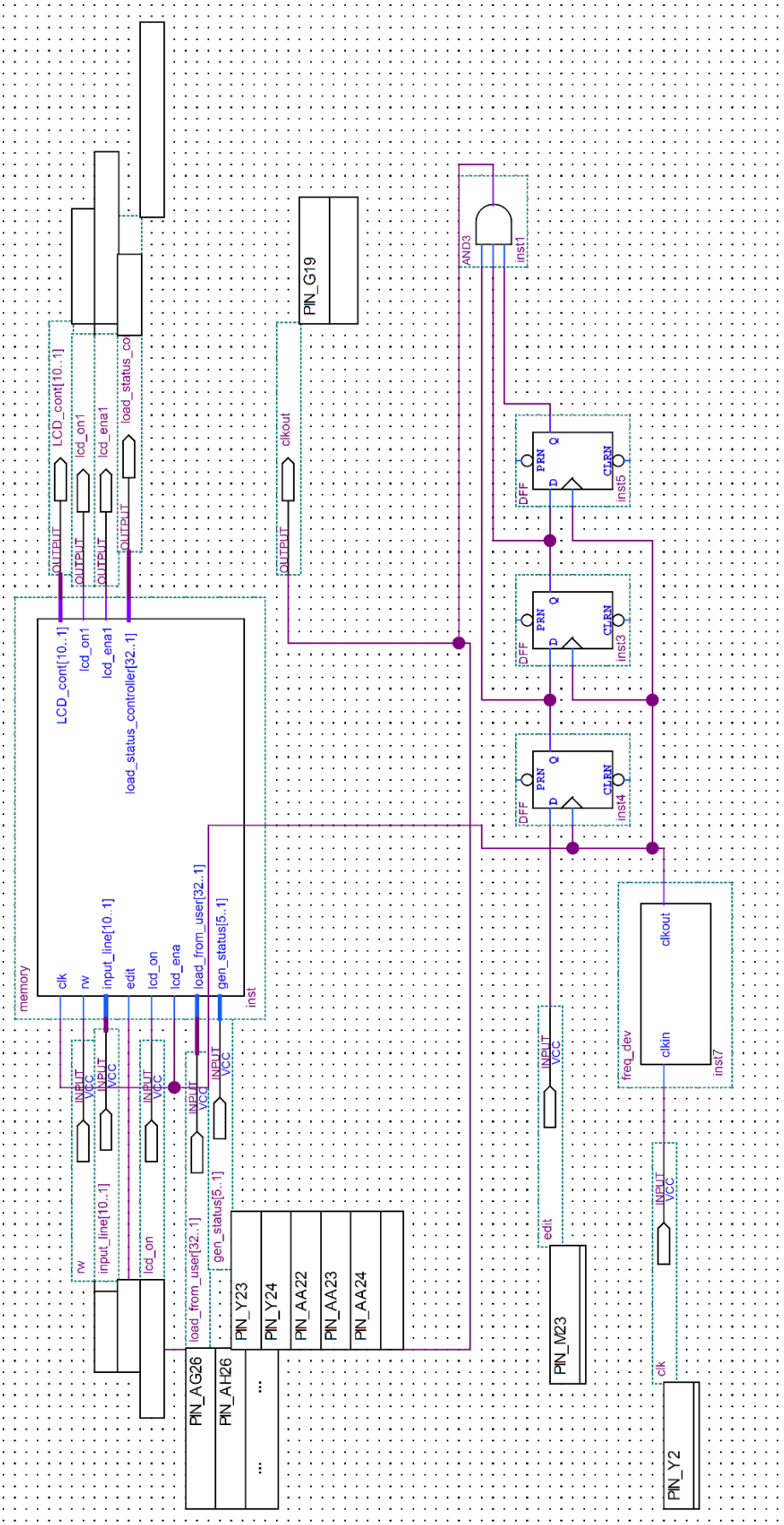

Figure 10. Schematic diagram of the implemented controller using Quartus.

Table 1. Example of Under Frequency Load Shedding (UFLS) Settings

Stage	Frequency	Time Delay	Load Shed
1	49.5 Hz	0.5 s	100 MW
2	49.0 Hz	2.0 s	300 MW

Table 2. Clock frequency of the implemented system with respect to number of loads

No. of loads	Frequency	Time Delay
32	10.24 KHz	0.1 s
64	40.96 KHz	0.1 s
128	163.84 KHz	0.1 s
256	655.36 KHz	0.1 s

Table 3. Priorities and power consumption of each load (arranged according device index)

Device name	Device Index	Devise Priority	Consumed Power
D1	1	25	10
D2	2	17	10
D3	3	26	70
D4	4	8	200
D5	5	24	50
D6	6	18	15
D7	7	23	65
D8	8	2	350
D9	9	19	20
D10	10	1	100
D11	11	12	15
D12	12	22	40
D13	13	6	5
D14	14	16	500
D15	15	7	25
D16	16	27	5
D17	17	13	100
D18	18	32	6
D19	19	9	35
D20	20	31	20
D21	21	15	90
D22	22	14	55
D23	23	30	10
D24	24	4	180
D25	25	20	70
D26	26	11	20
D27	27	3	40
D28	28	29	120
D29	29	10	110

D30	30	21	20
D31	31	28	90
D32	32	5	10

Table 4. Several cases to verify features of implemented LS controller (Rearranged according device priority).

Device name	Device Index	Devise Priority	Consumed Power	Case 1			Case 2			Case 3			Case 4		
				L_{IN}	L_{OUT}	conv	L_{IN}	L_{OUT}	conv	L_{IN}	L_{OUT}	conv	L_{IN}	L_{OUT}	conv
D10	10	1	100	0	0	0	1	100	100	1	100	100	1	100	100
D8	8	2	350	0	0	0	0	0	0	0	0	0	0	0	0
D27	27	3	40	0	0	0	0	0	0	0	0	0	0	0	0
D24	24	4	180	0	0	0	0	0	0	0	0	0	0	0	0
D32	32	5	10	0	0	0	0	0	0	0	0	0	0	0	0
D13	13	6	5	0	0	0	0	0	0	0	0	0	0	0	0
D15	15	7	25	0	0	0	0	0	0	0	0	0	0	0	0
D4	4	8	200	1	200	200	1	200	200	1	200	200	1	200	200
D19	19	9	35	0	0	0	0	0	0	0	0	0	0	0	0
D29	29	10	110	0	0	0	0	0	0	0	0	0	0	0	0
D26	26	11	20	0	0	0	0	0	0	0	0	0	1	20	20
D11	11	12	15	0	0	0	0	0	0	0	0	0	0	0	0
D17	17	13	100	1	100	100	1	100	100	1	100	100	1	100	100
D22	22	14	55	0	0	0	0	0	0	0	0	0	0	0	0
D21	21	15	90	0	0	0	0	0	0	0	0	0	0	0	0
D14	14	16	500	1	500	500	1	500	500	1	500	500	1	500	500
D2	2	17	10	0	0	0	0	0	0	0	0	0	0	0	0
D6	6	18	15	0	0	0	0	0	0	0	0	0	0	0	0
D9	9	19	20	0	0	0	0	0	0	0	0	0	0	0	0
D25	25	20	70	0	0	0	0	0	0	0	0	0	0	0	0
D30	30	21	20	0	0	0	0	0	0	0	0	0	0	0	0
D12	12	22	40	0	0	0	0	0	0	0	0	0	0	0	0
D7	7	23	65	0	0	0	0	0	0	0	0	0	0	0	0
D5	5	24	50	1	50	50	1	50	50	1	50	50	1	50	50
D1	1	25	10	0	0	0	0	0	0	0	0	0	0	0	0
D3	3	26	70	0	0	0	0	0	0	0	0	0	0	0	0
D16	16	27	5	0	0	0	0	0	0	0	0	0	0	0	0
D31	31	28	90	0	0	0	0	0	0	0	0	0	0	0	0
D28	28	29	120	1	120	120	1	0	0	1	0	0	1	0	0
D23	23	30	10	0	0	0	0	0	0	0	0	0	0	0	0
D20	20	31	20	0	0	0	0	0	0	1	20	0	1	20	0
D18	18	32	6	0	0	0	0	0	0	1	6	0	1	6	0
Power KVA				970	970	970	1070	950	950	1096	976	950	1136	996	970
				Required	suggested LS	Traditional LS	Required	suggested LS	Traditional LS	Required	suggested LS	Traditional LS	Required	suggested LS	Traditional LS

Total Load shed	---	---	---	---	---	---	---	120	146	---	120	146
No. of isolated loads	---	---	---	---	1	1	---	1	3	---	1	3
Unused power because of shedding	---	---	---	---	50	50	---	24	50	---	4	30